PATENT WATCH

By Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@umunhum.stanford.edu *with comments or questions.*

5,958,061

Host microprocessor with apparatus for temporarily holding target processor state

Filed: July 24, 1996 **Issued: September 28, 1999**
Inventors: Edmund Kell et al. **Claims: 22**
Assignee: Transmeta

Apparatus for use in a system having a microprocessor capable of executing a first instruction set to assist in running instructions of a guest instruction set that is translated to the first instruction set by the host processor. A store queue is included for temporarily holding memory store operations until determining that a sequence of translated instructions will execute without exception or error on the host processor. When a sequence of translated instructions generates an error, the memory store operations are eliminated.

5,956,753

Method and apparatus for handling speculative memory access operations

Filed: August 19, 1997 **Issued: September 21, 1999**
Inventors: Andrew Glew et al. **Claims: 31**
Assignee: Intel

A microprocessor in which speculative memory instructions access memory locations that may or may not be speculatable. The "speculatability" of these locations is stored with other data in the TLB. Depending on the result of a TLB access on behalf of a speculative memory reference, the speculative memory access may or may not be allowed to complete.

5,953,520

Address translation buffer for data processing system emulation mode

Filed: September 22, 1997 **Issued: September 14, 1999**
Inventor: Soummya Mallick **Claims: 16**
Assignee: IBM

A processor and methods for a microprocessor that has a native instruction set and emulates instructions of a guest instruction set. Native semantic routines emulate guest instructions. The semantic routines utilize native addresses. In response to a guest memory access instruction for emulation, the guest logical address is first translated into a guest real address, which is then translated into a native physical address. The instruction is then executed using native addresses.

5,950,012

Single chip microprocessor circuits, systems, and methods for self-loading patch micro-operation codes and patch micro-instruction codes

Filed: March 7, 1997 **Issued: September 7, 1999**
Inventors: Jonathan Shiell et al. **Claims: 67**
Assignee: TI

A microprocessor and methods of operating a system whereby, depending on the configuration of the system, one of a set of patches to microcode may be selected. The patch microcode is stored in a microprocessor-accessible memory and augments or replaces selected microcode stored in the microprocessor's ROM. A patch table associates microcode ROM addresses to patched addresses, so that accessing a patched microcode location will instead read the patched code. The microprocessor includes an instruction that configures the patches.

5,949,995

Programmable branch prediction system and method for inserting prediction operation which is independent of execution of program code

Filed: August 2, 1996 **Issued: September 7, 1999**
Inventor: Jackie Freeman **Claims: 13**
Assignee: none

A system and methods for inserting additional prediction operations into program code to predict behavior of a branch. The inserted code computes and stores values into a data storage that is then used by a predictor to predict the branch outcome.

5,949,994

Dedicated context-cycling computer with timed context

Filed: February 12, 1997 **Issued: September 7, 1999**
Inventors: Wayne Dupree et al. **Claims: 27**
Assignee: Dow Chemical

A dedicated context cycling microprocessor with individual sets of dedicated registers for each context is disclosed. Multiple I/O circuits each have a dedicated context. The microprocessor is intended to work with and control another microprocessor and an external memory system by handling the system I/O.

OTHER ISSUED PATENTS

5,960,466 *Computer address translation using fast address generator during a segmentation operation performed on a virtual address*

5,956,495 *Method and system for processing branch instructions during emulation in a data processing system*

5,953,512 *Microprocessor circuits, systems, and methods implementing a loop and/or stride predicting …*