PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@umunhum.stanford.edu *with comments or questions.*

5,999,727

Method for restraining over-eager load boosting using a dependency color indicator stored in cache with both the load and store instructions

Filed: June 25, 1997 **Issued: December 7, 1999**
Inventors: Ramesh Panwar et al. **Claims: 19**
Assignee: Sun

Methods for executing memory instructions in an out-of-order processor to ensure that memory operations occur in order. Load and store operations stored in the instruction cache are checked for load/store dependencies. Upon detecting a load/store dependency, the dependent instructions are marked with a color, indicating the load/store dependency between them.

5,995,749

Branch prediction mechanism employing branch selectors to select a branch prediction

Filed: November 19, 1996 **Issued: November 30, 1999**
Inventor: Thang Tran **Claims: 22**
Assignee: AMD

Branch prediction hardware and methods that store branch selectors, which correspond to instruction bytes in an instruction-cache line. The branch selectors identify a branch prediction to be chosen if the corresponding instruction byte is indicated by the offset of the fetch address for the cache line. Instead of comparing pointers to the branch instructions with the offset of the fetch address, the branch prediction is selected by decoding the offset of the fetch address and choosing the corresponding branch selector.

5,995,746

Byte-compare operation for high-performance processor

Filed: June 6, 1996 **Issued: November 30, 1999**
Inventors: Richard Sites et al. **Claims: 63**
Assignee: DEC

Methods of operation and a microprocessor that operates to produce a multiple-portion data register as the result of comparing two multiple-value registers and, based on this comparison and a third value, a fourth value is produced. The method consists of comparing each portion of the first register to a corresponding portion of the second register; generating a result value for each comparison in the second register; and generating a final value, where each portion of the final value is a function of a corresponding result portion in the second register and a third register.

5,974,240

Method and system for buffering condition code data in a data processing system having out-of-order and speculative instruction execution

Filed: June 7, 1995 **Issued: October 26, 1999**
Inventor: Kin Shing Chan **Claims: 10**
Assignee: IBM

Methods for simultaneously executing instructions that modify a condition-code register are disclosed. When instructions that modify certain fields in the condition-code register are simultaneously dispatched, each instruction is assigned a condition-code register-rename buffer. The condition-code bits of the instructions are written into the corresponding condition-code rename buffer. When the instructions are retired in order, the appropriate fields in the corresponding condition-code register-rename buffer are copied into the architectural condition-code register.

5,966,544

Data speculatable processor having reply [sic] *architecture*

Filed: November 13, 1996 **Issued: October 12, 1999**
Inventor: David Sager **Claims: 13**
Assignee: Intel

A microprocessor having a replay architecture that allows the processor to execute instructions using data speculation. A delay unit makes and holds a copy of an instruction during data-speculative execution. Upon determining that the instruction used incorrectly speculated data, the instruction is "replayed" by selecting the delay unit as the source of the next instruction and by executing the instruction with the correct, nonspeculative data.

5,963,744

Method and apparatus for custom operations of a processor

Filed: April 30, 1997 **Issued: October 5, 1999**
Inventors: Gerrit Slavenburg et al. **Claims: 10**
Assignee: Philips

A computer system using a processor with special-purpose SIMD instructions. The SIMD instructions operate on M-bit-wide data-input registers, each containing multiple N-bit values. Resultant intermediate values are clipped to N-bit results, packed, and stored into an M-bit result register.

OTHER ISSUED PATENTS

5,995,743 *Method and system for interrupt handling during emulation in a data processing system*

5,983,256 *Apparatus for performing multiply-add operations on packed data*

5,966,530 *Structure and method for instruction boundary machine state restoration*