Cahners
MICROPROCESSOR REPORT
www.MPRonline.com
THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

QED's RM7000A Gets Faster, Cooler

Process Shrink to 0.18 Micron Will Boost Frequency to 450MHz

By Tom R. Halfhill {4/3/00-05}

Squeezing more life out of a four-year-old core, Quantum Effect Devices (QED) is producing a new version of its 64-bit MIPS-compatible RM7000 processor in a 0.18-micron process from TSMC (Taiwan Semiconductor Manufacturing Co.). The new RM7000A will run up to 50% faster while consuming 66% less power than its predecessor. QED will soon follow with the RM7000B, which uses 0.15-micron transistors on the same-size die, boosting clock frequencies to 500MHz.

Samples of the RM7000A are available now at 400MHz, with production scheduled for 3Q00. QED plans to produce a 450MHz part in 4Q00. By then, the company hopes to have samples of the 500MHz RM7000B, which will enter production in 1H01. In contrast, today's fastest RM7000 runs at 300MHz and is manufactured in a 0.25-micron four-layer-metal process. The new 0.18- and 0.15-micron processes have six metal layers (aluminum).

All these chips could run significantly faster if they weren't restrained by a relatively short five-stage pipeline. It didn't seem like a handicap when QED announced the RM7000 at Microprocessor Forum in 1996 (see *MPR 10/28/96-09*, "RM7000 Strong on Cost/Performance"), but since then superpipelines delivering higher frequencies have become all the rage.

To address that issue, QED is working on a next-generation MIPS-compatible core that's code-named Apollo. It will have a slightly longer pipeline, probably seven stages, among other improvements. No introduction date has been announced, but we expect Apollo to appear first as the core in a highly integrated chip sometime next year, followed by a discrete version of the CPU later in 2001. QED is also working on a multiple-core version that's code-named Gemini.

Feature	RM7000A QED	RM7000B QED	RM7000 QED	RM5261 QED	RC64575 IDT	RC5000 IDT	VR5432 NEC
64-Bit Core	RM7000	RM7000	RM7000	RM5000	RC5000	RC5000	VR5400
Bus Width	64b	64b	64b	64b	32/64b	64b	32b
Max Freq	450MHz	500MHz	300MHz	266MHz	250MHz	250MHz	167MHz
I-Cache	16K	16K	16K	32K	32K	32K	32K
D-Cache	16K	16K	16K	32K	32K	32K	32K
L2 Cache	256K	256K	256K	Off-chip	Off-chip	Off-chip	Off-chip
L2 Interface	On-chip	On-chip	On-chip	No	No	Yes	No
L3 Interface	Yes	Yes	Yes	No	No	No	No
Cache Locking	Yes	Yes	Yes	Yes	Yes	No	Yes
Pin Count	304	304	304	208	208	272	208
IC Process	0.18µ 6M	0.15µ 6M	0.25µ 4M	0.25µ 4M	0.25µ 3M	0.35µ 3M	0.25µ 3M
Dhrystone 2.1	675 mips*	750 mips*	450 mips	345 mips	330 mips*	333 mips*	347 mips*
Power (typ)	2.5W	1.2W*	7.5W	4.2W	4W	8W	2.5W
Price (10K)	$225	n/a	$130	$48	$52	$99	$30
Availability	4Q00†	1H01	Now	Now	Now	Now	Now

Table 1. The most distinguishing feature of QED's RM7000-series processors is a 256K on-chip L2 cache; the new RM7000A consumes much less power. *MDR estimate. †QED plans to ship 350- and 400MHz versions of the RM7000A in 3Q00. n/a = not available.

Price & Availability

QED's RM7000A is sampling now at 350MHz and 400MHz and is scheduled to enter production in 3Q00. It will be priced at $135 (350MHz) and $175 (400MHz) in 10,000-unit quantities. The 450MHz chip is scheduled to enter production in 4Q00 and sell for $225. QED says samples of the 500MHz RM7000B will be available in 4Q00 and production will begin in 1H01. QED has not yet announced a price for that part.

New Process Shrinks Die By 38%

In almost all respects, the RM7000A and RM7000B are identical to the RM7000. Their most notable features are a 256K on-chip secondary cache, an integrated controller for an optional L3 cache, and superscalar pipelines that can execute any pair of integer or floating-point instructions in parallel. (R5000-based MIPS processors have more limited superscalar cores—they can issue only an integer and a floating-point instruction in parallel, not pairs of the same data types.) As with late-model RM7000 chips, the RM7000A and RM7000B have 64-entry TLBs instead of the 48-entry TLBs in early RM7000 parts.

Moving to a 0.18-micron process shrinks the RM7000A's die size to 50mm^2, compared with 90mm^2 for the RM7000. The RM7000B's die will also be 50mm^2, because it uses a hybrid process with 0.15-micron (L-effective) transistors but 0.18-micron interconnects. Eventually, an optical shrink to 0.15 micron will reduce the RM7000B's die size as well.

The 1.8V RM7000A consumes only 2.5W (typical) at 400MHz, compared with 7.5W for a 300MHz RM7000. That's based on a Dhrystone 2.1 measurement; the chip's maximum power consumption when running more demanding software is only 3.5W at 400MHz. When lower power consumption is more important than higher performance, the RM7000A can run at 1.65V and 300MHz while burning only 1.5W, according to QED. At 450MHz, typical power consumption rises to about 2.8W.

QED's 10,000-unit prices for the RM7000A are $225 (450MHz), $175 (400MHz), and $135 (350MHz). As Table 1 shows, those tickets put the RM7000A in the same front-row seats as IDT's 300MHz RC5000, another 64-bit MIPS-compatible processor for high-performance embedded applications. At any clock speed, the RM7000A is significantly more expensive than IDT's new RC64574 and RC64575, which run at 300MHz and 333MHz, respectively (see *MPR 8/23/99-04*, "IDT Expands Embedded MIPS Family").

The IDT processors have twice as much primary cache as the RM7000A, and the '574 and '575 also have some multimedia instructions not supported by QED's core. But the IDT processors lack on-chip L2 caches and the ability to execute two instructions of the same data type in parallel. Also, the RM7000A's integrated cache controller allows system designers to add an L3 cache—not an option on the IDT processors—and the QED chip consumes much less power.

None of these chips is suitable for a low-power embedded application, but reduced power consumption simplifies the cooling problems of switches and routers, which have many densely packed line cards.

New Competition Is a Threat

QED is targeting the RM7000A and RM7000B primarily at routers, access concentrators, and other network-infrastructure devices—applications that can use the on-chip L2 cache and optional L3 cache for storing routing tables and other performance-critical data structures closer to the core. In that market, RISC vendors such as QED face increasing competition from a new breed of network processors whose architectures are specifically designed for networking.

The RM7000A and RM7000B don't attempt to compete with network processors by processing packets in the main datapath of a router. Instead, they're designed to execute control code and other system-management tasks. But some network processors try to handle those jobs as well. Over the next few years, the insatiable demand for more bandwidth and throughput will force RISC vendors to respond in more specific ways than shrinking die sizes and boosting clock speeds. To stay competitive in the long run, enhancements at the architectural or microarchitectural levels are necessary. QED's next-generation Apollo and Gemini designs will almost certainly address those concerns better than the RM7000A and RM7000B. In the meantime, these swifter versions of the time-proven RM7000 will hold down the fort. ◇