Cahners
MICROPROCESSOR REPORT
www.MPRonline.com
THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

MIPS Joins Forces With TSMC

By Tom R. Halfhill {4/3/00-11}

MIPS Technologies has formed a partnership with TSMC (Taiwan Semiconductor Manufacturing Co.) to make prehardened versions of its soft embedded-processor cores. Among other things, the deal gives customers the option of paying a design-use fee instead of the higher cost of a MIPS architectural license while saving the time and trouble of porting a soft core to an IC process themselves.

TSMC is the world's largest foundry, with 11 fabs in operation and 3 more under construction—enough capacity to ship 3.5 million 8-inch wafers this year. TSMC also offers design services, including extensive third-party libraries of intellectual property (IP) that have already been verified on the company's fabrication processes. The MIPS-TSMC partnership could allow customers to accelerate their development schedules for system-on-a-chip (SOC) devices and reduce the risk of integrating IP from multiple providers.

The arrangement resembles an alliance between MIPS and Chartered Semiconductor announced last year (see *MPR 7/12/99-en*, "MIPS and Chartered Form Unique Partnership"). That deal allows Chartered to market some prehardened MIPS cores under the terms of a simplified license. But there are three key differences between the Chartered alliance and the new arrangement with TSMC:

- TSMC can manufacture prehardened versions of MIPS32- and MIPS64-based cores, while Chartered can offer only MIPS32 cores under the simplified license. (If the customer has a regular MIPS license, Chartered can manufacture any MIPS core.)
- The licensing terms with TSMC are more flexible, because customers can negotiate with MIPS for a design-use license or a broad architectural license. The simplified MIPS license with Chartered is a design-use license that's less negotiable.
- MIPS will handle the marketing and technical support for the TSMC-hardened cores, while Chartered handles the marketing and support for its hardened versions of the cores.

On the other hand, obtaining a MIPS core through Chartered should be quicker and easier, because customers don't have to pay an upfront license fee or negotiate with MIPS. The simplified agreement offered by Chartered is more like a 1040-EZ version of a long-form MIPS license—and bartering for a broad architectural license can be a lengthy process. In either case, whether customers license a MIPS core through TSMC or Chartered, they'll pay volume-based royalties on the chips to MIPS.

Initially, TSMC will manufacture a hardened version of the MIPS32 4Kc in a 0.18-micron process. It's scheduled to be available in 3Q00. In 4Q00 or 1Q01, TSMC will manufacture a hardened version of the MIPS64 20Kc, a 64-bit core that MIPS will officially announce at Embedded Processor Forum in June. In the future, TSMC will port the cores to a 0.15-micron process, which is ready for production now.

One disadvantage of using a prehardened core instead of a synthesizable model is that customers have less control over the design. MIPS and TSMC decided to offer the 4Kc first because they expect it to be the most popular version of the three 4K-series cores (see *MPR 5/31/99-05*, "Jade Enriches MIPS Embedded Family" and *MPR 10/6/99-en*, "MIPS32 4Km Core Has Fast MAC"). The 4Kc has a 32-entry TLB and a single-cycle 32 x 16 multiplier, and TSMC will configure it with a 16K instruction cache

and a 16K data cache—twice as much cache as MIPS suggests for a "typical" application.

The TSMC partnership dovetails with MIPS's business strategy of trying to earn more revenues from royalties while depending less heavily on upfront license fees. By making it easier for potential customers to obtain drop-in cores under various licensing terms, MIPS hopes to broaden the adoption of its embedded cores. Competitors such as ARM and ARC Cores have also been aggressively licensing their embedded cores, creating a snowball effect of royalties as products based on those cores win sales in the marketplace.