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Extreme Lithography

Intel Backs EUV for Next-Generation Lithography

By Keith Diefendorff {6/19/00-01}

Working at the very boundary between theoretical physics and practical engineering, scientists at Lawrence Livermore, Sandia, and Lawrence Berkeley National Laboratories appear to have beaten into submission many of the obstacles standing in the path of extreme-ultraviolet radiation's becoming the industry choice for next-generation lithography (NGL). By calling on technology they developed for the "Star Wars" space-based ballistic-missile-defense system, spy satellites, and the Hubble Space Telescope, these scientists believe they can use "light" in the extreme-ultraviolet (soft x-ray) region of the electromagnetic spectrum to image transistors as small as 20 nanometers. (Below 20nm, silicon transistors cease to operate normally.)

The extreme-ultraviolet lithography (EUVL) effort at the three labs—collectively called the Virtual National Laboratory (VNL)—is funded entirely by the private sector under a $250 million cooperative research and development agreement (CRADA) between the U.S. government and a limited liability company called EUV LLC. Intel established EUV LLC in 1997, along with AMD and Motorola, to sponsor EUVL development and commercialization; recently, Infineon and Micron also joined the consortium.

Chuck Gwyn, program director at EUV LLC, says the company will transfer the technology developed by the VNL to semiconductor-equipment manufacturers to assist those companies in building commercial steppers and associated equipment. In return for their investments, EUV LLC members are granted first rights of refusal on the tools those equipment manufacturers produce. Members will also receive royalties on the sales of tools that embody EUV LLC intellectual property. The VNL has already amassed a large body of IP; Don Sweeney, CTO of the VNL, says more than 90 patents have been filed to date. Perhaps the greatest benefit of EUV LLC membership, however, will be early access

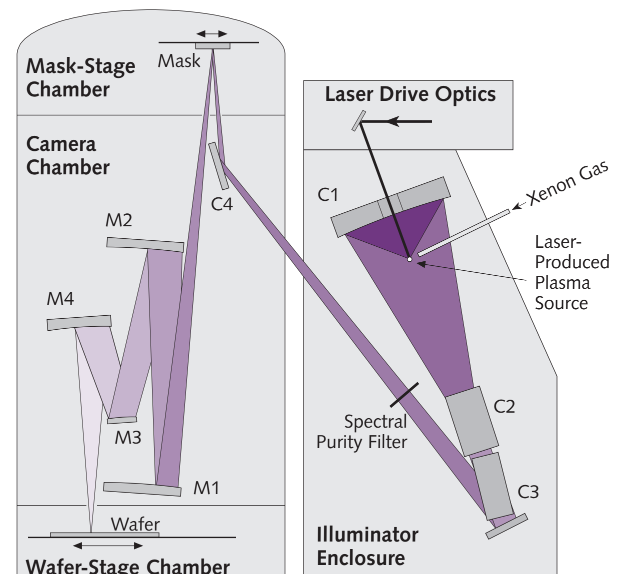

Figure 1. EUV light is generated from a 45eV plasma created when a 1,700W pulsed YAG solid-state laser illuminates a supersonic jet of xenon gas. The EUV light is collected and focused on a 4x reflective mask by a series of condenser mirrors (C1–C4). The mask image is projected onto the wafer by a 4x reduction camera (M1–M4) while the mask and wafer are simultaneously scanned. The entire operation takes place in high-vacuum environmental enclosures.

to VNL know-how, an advantage that could give member companies a two-year head start on the rest of the industry.

Not a Simple Problem

The problems of imaging ever-smaller features onto a wafer are many and difficult. In fact, Intel Fellow Mark Bohr, director of process architecture and integration at Intel, says lithography is the single largest technology problem facing Intel in the future. Gwyn notes that drawing 70nm features onto an integrated circuit is the equivalent of drawing features the size of a quarter onto the surface of the earth from the height of an orbiting space shuttle—190 miles. Such resolution requires imaging systems well beyond the current state of the art.

The resolution of an optical imaging system (i.e., a camera, such as is contained in a stepper) is given by the simple formula $k_1\lambda/NA$, where λ is the wavelength of the light source and NA is the numerical aperture of the lens system. Current production steppers operate at a wavelength of 248nm and typically have numerical apertures of 0.6. The k_1 parameter is determined empirically as the value that gives the desired control over critical dimensions (CDs) within an acceptable manufacturing window; it accounts for factors such as camera performance, resist contrast, and etch characteristics. A k_1 of 0.5 is generally accepted as the diffraction-limited resolution (Raleigh criterion) of an optical system, but values of 0.6 or more are preferable for greater latitude in high-volume manufacturing. Manufacturers can, however, push steppers to higher resolution using k_1 values considerably less than 0.5, at the price of some loss of control over CDs, some magnification of mask errors, and a few other undesirable effects.

From this formula, it is apparent that decreasing the wavelength of the light source, or increasing the numerical aperture of the lens system, can increase resolution. Increasing NA, however, rapidly sacrifices depth of focus. Depth of focus, the distance along the optical axis that the final image is in sharp focus, decreases linearly with wavelength but inversely with the square of the numerical aperture ($DoF = k_2\lambda/NA^2$). Depths of field of 0.5µm or greater are preferable for volume manufacturing, but 248nm steppers imaging 0.18-micron features, at $k_1$and $k_2$values of 0.45, offer a depth of focus of only about 0.3µm.

Reducing the wavelength to 193nm, as is planned for next-generation steppers, will allow k values to be relaxed to 0.55, at a NA of 0.6, or, alternatively, allow depth of focus to be extended to 0.4µm, at a reduced NA of 0.45. Resolution-enhancement techniques (RETs), such as phase-shift masks, off-axis illumination, and optical-proximity correction, can be used to push resolution somewhat further, or to increase the effective depth of focus. But these techniques are expensive, and they can be difficult to manage in volume-manufacturing environments.

According to SEMATECH (*www.sematech.org*)—the 13-company consortium that serves as the focal point for much of the industry's advanced-process-technology work and the organization that maintains the *International Technology Roadmap for Semiconductors* (ITRS99)—248nm steppers will take the industry through the 0.18-micron generation, and 193nm steppers will get it comfortably through 0.13 micron. Silicon Valley Group says its new 193nm 0.75-NA Micrascan-V can pattern dense lines and spaces down to 0.10-micron without phase-shift masks, but most of the industry is focused on 157nm steppers for the 0.10-micron and 70nm generations. Progress is slow, however, and there is some doubt that commercial 157nm steppers will be ready by the time they are needed, around 2003.

Even if 157nm steppers pan out for the 70nm generation, it is universally agreed that going beyond this level will require a next-generation lithography—one that uses radiation of at least an order-of-magnitude shorter wavelength. Such short wavelengths would allow much higher resolution, even with lower numerical apertures.

The problem with short-wavelength light is that most materials absorb it strongly and reflect it poorly. Even 193nm wavelengths are a problem: the only material capable of transmitting and refracting the light from a 193nm argon-fluoride excimer laser is calcium fluoride, which, at a price of $10,000 per kilogram, makes for very expensive lenses. (Typical 193nm steppers require up to 50kg of calcium fluoride, although the new Micrascan-V requires only 2kg.) The opacity and absorption problems get worse at shorter wavelengths: no known material is transparent to light much below a wavelength of 157nm.

As a result, systems that use electromagnetic radiation with order-of-magnitude shorter wavelengths cannot use refractive optics (lenses)—only specially designed reflective optics (mirrors) will work. At these ultrashort wavelengths, even air is completely opaque. This means that next-generation lithography must be carried out under high vacuum, complicating the design of NGL systems.

Which NGL Will It Be?

Three years ago, SEMATECH listed five candidates for NGL: X-ray lithography (XRL), ion-projection lithography (IPL), e-beam direct write (EBDW), electron-projection lithography (EPL), and extreme-ultraviolet lithography (EUVL). At that time, SEMATECH considered EUVL the least likely candidate to succeed. Since that time, the situation has changed dramatically and EUVL has now jumped into the lead, although industry support is strong behind EPL as well (see *MPR 5/1/00-01*, "IBM Paving the Way to 0.10 Micron").

EUVL has taken the lead primarily on the strength of an alpha-class prototype tool, called the engineering test stand (ETS), which the VNL and EUV LLC announced on May 11. The ETS is a complete 13.4nm stepper capable of imaging 70nm features on a 200mm wafer at a k_1 of 0.52 and a depth of focus of 0.7µm, using a numerical aperture of 0.1.

The ETS consists of several major subsystems: a light source with condenser optics to collect the light and illuminate the mask; a mask-transport stage to scan the mask; a reflective 4x mask (which holds the circuit image); a 4:1-reduction camera to project the mask image onto the wafer; and a wafer-transport stage to scan the wafer in synchrony with the mask and step the wafer into position to accept the next image. Figure 1 shows a schematic diagram of the ETS. Each of its subsystems requires precision greater than that of any equipment used in manufacturing today.

A Laser-Produced Plasma (LPP) Source

Since 13nm radiation is strongly absorbed by all materials, the EUV light source must be sufficiently intense to allow for large losses in the optical path while still casting enough light on the wafer for the short exposure times needed for high wafer throughput. At the same time, the light source must start out extremely small, essentially a point source, to simplify the optics and provide even illumination. To achieve these objectives, the VNL scientists used a powerful 1.06µm laser to excite a continuous jet of inert xenon gas, creating a hot plasma that releases its energy in the EUV portion of the spectrum.

The ETS laser is a pulsed (6,000Hz) solid-state ytterbium-aluminum-garnet (YAG) laser, built by TRW, that produces about 1,700W of optical power. The 1,700W laser yields about 10W of EUV power from the plasma in the 2.5% spectral bandwidth around 13.4nm. The EUV light radiates in all directions from the approximately spherical 150µm-diameter source point. A six-petal condenser mirror (C1), which intercepts a solid angle of 1.8 steradians around the source, collects about 27% of this EUV energy and directs it to grazing-incidence flat mirrors (C2) that rotate and converge the six beams. Slightly convex grazing-incidence mirrors and a convex normal-incidence mirror in the C3 complex bend and relay the beam through a spectral-purity filter and toward C4, a toroidal grazing-incidence mirror that produces the final 96mm-long arc that illuminates the mask. This arc is a portion of a 30° ring field that is uniformly illuminated to within ±1%. About 1W of 13.4nm EUV light reaches the mask. Figure 2 shows an engineering prototype of the ETS light source and C1 assembly.

A large number of difficult challenges had to be overcome to build the ETS light source. First, the main condenser mirror, being near the source, is subject to distortion from heat. To minimize this distortion, the C1 assembly is water cooled. Each petal is a three-inch-thick single-crystal-silicon ingot. Silicon is used rather than traditional glass mirror blanks, because its higher thermal conductivity reduces stress-induced distortion created by uneven temperature distribution between the hot plasma source and the cool heatsink.

Another serious problem is deterioration of C1's reflective surface due to particulate debris from the light source. The invention of the clean xenon source in 1994 reduced the debris problem by five orders of magnitude over the initial (1991) design, which employed a solid gold laser target. But erosion of nozzle material by the supersonic xenon gas jet and sputtering of nozzle material by the 45eV plasma are still problems. Since the first xenon source, the problem has been reduced by an order of magnitude, using improved nozzle materials. C1 lifetime now stands at better than 10^9 pulses (before reflectivity is reduced by 10%). The goal for the ETS is more than 10^{10} pulses, which newly developed techniques are expected to deliver. Even at that rate, however, condenser lifetime will be only about six months. As a result, the C1 and C3 mirror assemblies were designed to be prealigned and easily replaceable. The mirrors themselves, however, are not repairable; they must be replaced, thus creating some really neat high-tech souvenirs.

A third problem was mechanical instability. All 19 mirrors in the condenser assembly must retain their relative positions to within better than 60µm. To meet this specification, the entire condenser assembly had to be mechanically isolated from the environmental chamber so that, for example, vibration from the vacuum pumps would not affect the mirrors.

A Really High Resolution Camera

In the ETS, a one-quarter-size image of the mask is printed on the wafer using a four-mirror (M1–M4) projection-optics system (the camera) with a numerical aperture of 0.1. The mask itself is a flat mirror on which a 500nm-thick

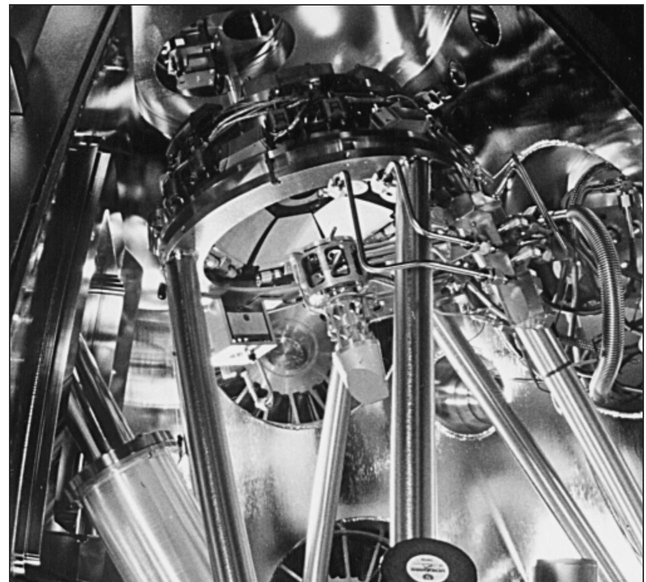

Figure 2. This engineering prototype of the engineering test stand (ETS) illuminator shows the LPP light source and the C1 condenser assembly (top center). Small trapezoidally shaped doors protect the six C1-mirror petals when the ETS is not in operation. The entire condenser weldment, which also holds C2 and C3, is isolated from its environmental chamber to eliminate motion and vibration from the vacuum pumps. (Photo courtesy of Sandia National Lab)

absorber film is deposited; the circuit pattern is formed in the film by reactive ion etching.

The ETS camera light path is shown schematically in Figure 3. The four-element design was selected because of its ability to simultaneously satisfy the ETS goals of 4:1 reduction ratio; telecentricity at the wafer; low field curvature; low image distortion; and near-normal incidence angles on the mirrors, which simplify the mirror coatings.

The optic cells that hold the mirrors are positioned with high dimensional stability relative to each other by a welded Super Invar structure; an early prototype of the camera is shown in Figure 4.

The camera optics are a marvel of engineering perfection. The total wavefront error across the surface of each individual ETS-camera mirror is currently less than 0.5nm rms, and the final mirror set will be 0.25nm. Such an accurate figure is necessary to produce a composite wavefront error at the exit pupil of the camera of better than λ/14, which is the requirement for diffraction-limited performance according to Marechal's criterion.

This precision is especially amazing, considering that three of the mirror surfaces (M1, M2, and M4) are aspheric because of the off-axis design needed to achieve a clear light path, illustrated in Figure 3, and because of the need to correct aberrations at each interface. The key enabler for creating these accurate figures was the development of an interferometer with a wavefront error of λ/300 (0.044nm, the size of one hydrogen atom). This tool can make accurate absolute measurements of the mirrors' aspheric-figure errors, rather than the relative errors measured by previous interferometers.

Not only must the mirrors be precisely figured, their surfaces must be extremely smooth and free of defects. Any roughness or defects in these surfaces scatter light, creating a background illumination (flare) that reduces image contrast. Flare increases as $1/\lambda^2$, making it a far larger problem at EUV wavelengths than at DUV wavelengths. Worse yet, variation in flare across the optical field creates nonuniformity in the critical dimensions printed on the wafer. ETS mirrors have a midspatial-frequency roughness of about 0.25nm rms and will be improved to 0.20nm on the final mirror set.

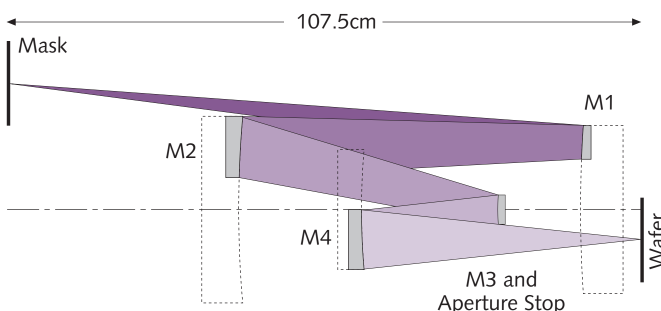

Figure 3. This scale diagram shows the folded light path of the four-mirror projection-optics assembly (the camera) used in the ETS. The system is designed to maintain near-normal incidence angles to simplify mirror coatings. To achieve a clear light path, only small portions (gray) of the otherwise large mirrors are implemented. All mirror surfaces are aspheric except M3, which also includes the aperture stop. The design is telecentric at the wafer.

Reflecting the Unreflectable

Near-perfect mirror surfaces that reflect EUV light with high efficiency are critical to the success of the ETS, because optical throughput is proportional to mirror reflectance raised to the seventh power. But high reflectance for near-normal-incidence mirrors is a serious challenge at EUV wavelengths.

The solution devised by the VNL team is a distributed Bragg reflector consisting of a stack of alternating quarter-wavelength layers of molybdenum and silicon, as Figure 5 shows. In this type of reflector, a small portion of the incident light is reflected from each silicon surface; the thickness of the layers causes the reflected waves to interfere constructively. Currently, 40 layer pairs are used to coat each mirror; more layers would increase reflectance somewhat, but the returns diminish for more layers, and the gain would be offset by the accumulation of surface errors. With the use of this type of multilayer coating, individual mirror reflectance of 70% has been achieved at the wavelength of interest, producing a total optical throughput of about 8% through all seven near-normal-incidence mirrors in the ETS, including the mask.

The layers are deposited on the mirror substrates by a DC-magnetron sputtering system. Mirror substrates are mounted face down on a platter that is swept in a circular motion across two 100–400W sputtering sources (one for moly, one for silicon) located 180° apart. This orientation allows the tool to deposit one bilayer each rotation; the

Photo by Keith Diefendorff

Figure 4. This photo shows the M2, M4, and M3 mirrors (left to right) in an early prototype of the four-mirror ETS camera. The optic cells are designed to hold the mirror without imparting any stress that could distort the mirror figure. The optic cells are held in precise relative position by a rigid Super Invar weldment.

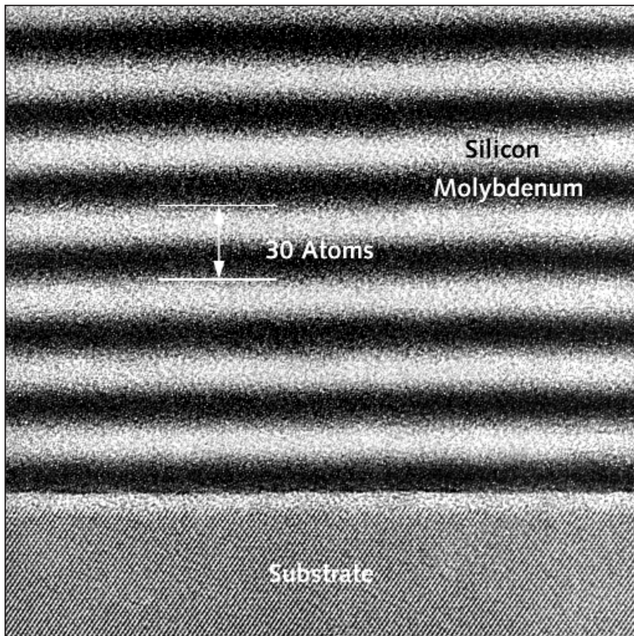

Figure 5. Each of the seven normal-incidence mirrors (including the mask) in the ETS is coated with 40 bilayers of molybdenum and silicon that are λ/2 (30 atoms) thick, creating a distributed Bragg reflector. Total reflectance at 13.5nm is 70%. (Source: Lawrence Livermore Lab)

rotation rate of the platter is precisely controlled to adjust layer thickness. During plating, each mirror substrate is spun rapidly about its own axis to assure a uniform coating. The entire operation is performed under high vacuum (10^{-7} Torr).

The coatings on all mirrors in a given system must be identical, so that the peak-reflectance wavelength of each is precisely aligned for maximum optical throughput. The VNL scientists have determined that the most practical way to achieve the required match is to coat all mirrors simultaneously. For this purpose, a large magnetron deposition chamber, shown in Figure 6, is now being tested at Lawrence Livermore. Figure 7 shows a finished M4 mirror from that system.

Particles and defects on the surface of the mirror substrate present a continuing problem. Such defects are especially problematic on the mask, because the mask, unlike other mirrors, is always in sharp focus. Thus, any mask defect is faithfully reproduced in every chip on the wafer. The VNL is pursuing mask-defect mitigation on two fronts: defect reduction and defect smoothing. The project goal is to eliminate all process-added defects down to 55nm in size and to smooth over defects smaller than that.

ETS masks have an active area of $135cm^2$ (the mask is a rectangle 96 x 130mm) and are built on 200mm epitaxial silicon wafers with raw defect densities less than 0.02 defects/cm^2 (for 80nm or larger defects). To minimize process-added defects, wafers are robotically loaded, using class-1 SMIF (standard mechanical interface) pod equipment, into a low-defect ion-beam deposition tool, shown in Figure 8, for coating. Recently, process-added defect densities of 0.011 defects/cm^2 (for 100nm or larger defects) have been achieved, but total defect densities of better than 0.003 defects/cm^2 are required to achieve 70% mask yield for a 25 x 25mm die. To achieve this milestone, extensive defect detection, characterization, and reduction efforts are under way.

Defect smoothing is accomplished by first coating the mask substrate with a buffer layer optimized to smooth defects and then building the multilayer coating over it, using a continuous process wherein the ion-beam energy and sputtering angle are gradually shifted from optimal smoothing to optimal reflectivity. Currently, defects are

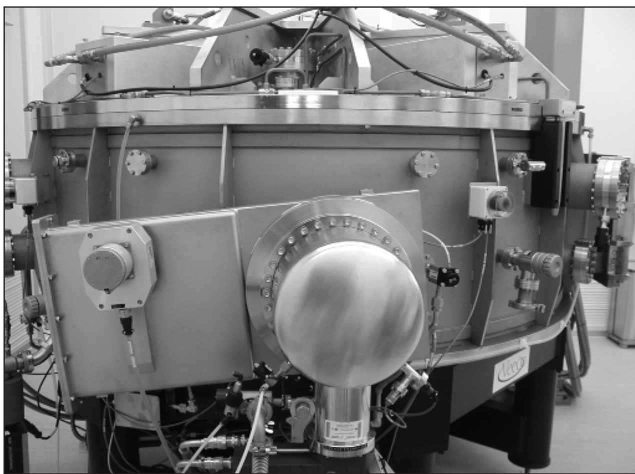

Photo by Keith Diefendorff

Figure 6. This large DC-magnetron sputtering source is being used at Lawrence Livermore Lab to coat all ETS mirrors simultaneously, a procedure that is required to get precisely matched peak-reflectance-wavelength characteristics for maximum optical throughput.

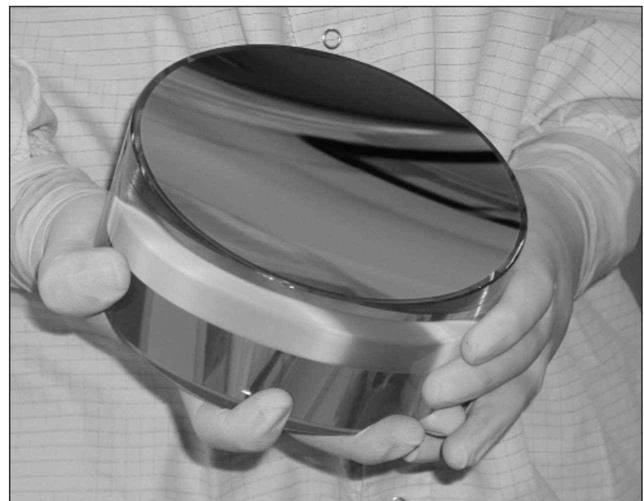

Photo by Keith Diefendorff

Figure 7. This photograph shows a polished and coated M4 mirror from the ETS camera. For people who appreciate ultrahigh precision, the mirror is a thing of beauty.

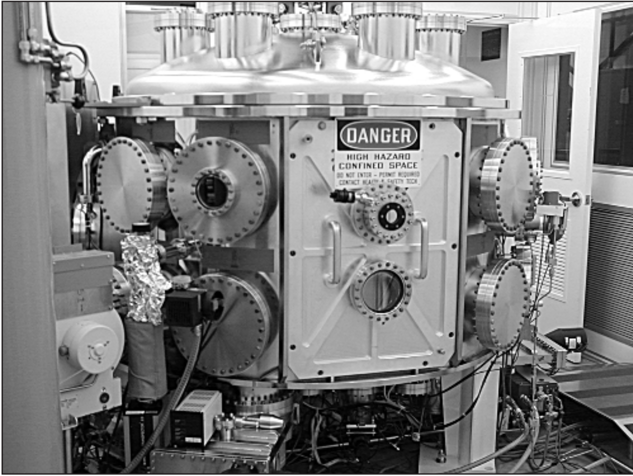

Photo by Keith Diefendorff

Figure 8. The DC-magnetron is okay for mirrors, but a much cleaner ion-beam sputter deposition tool is required for coating masks. Mask blanks (200mm silicon wafers) are robotically shuttled in and out of the tool using a class-1 SMIF pod system, which is located off to the left in a class-100 clean room.

being successfully eliminated down to about 90nm and smoothed over up to about 30nm. The VNL expects its defect reduction and defect smoothing efforts to converge on the 55nm goal by 2003.

Eliminating Gravity and Friction

The ETS is a step-and-scan system similar to that used in today's DUV optical steppers. In these systems, a wafer is first positioned to print one die or one reticle-size image (reticles sometimes contain more than one die image). The mask is then mechanically scanned in one dimension across the light source, which is a thin stripe of light that spans the width of the reticle. The mask image is projected through a camera onto the wafer, which is scanned in synchrony with the mask, but at a rate slower than the mask by exactly the reduction ratio of the camera, normally 4:1. When one scan is complete, the wafer is stepped to the next position, and another mask image is scanned onto it in the same manner; this step-and-scan process repeats until the wafer is filled.

The difference between the step-and-scan process for EUVL and DUVL is primarily one of precision. EUVL steppers require mechanical positioning and scanning accuracy far beyond that required in manufacturing today. For this, the VNL scientists have developed vacuum-compatible magnetically levitated reticle and wafer stages, along with ultraprecise position-measuring (metrology) devices and sophisticated feedback and control systems to position and move the stages.

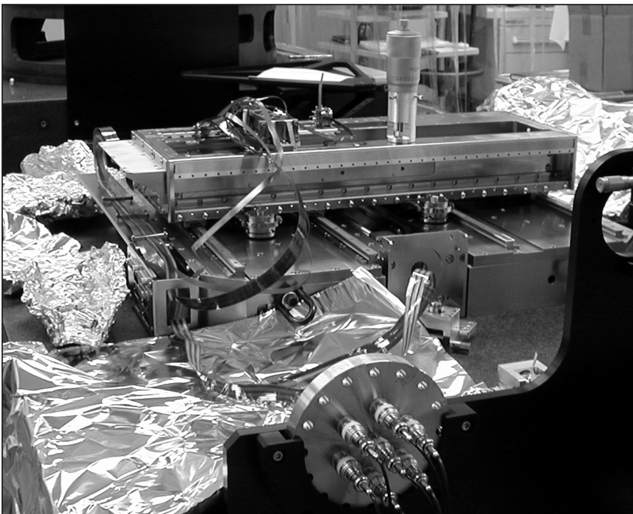

Photo by Keith Diefendorff

Figure 9. This photograph shows the maglev wafer stage being assembled at Sandia National Lab just before integration into the camera environmental enclosure. The platen and electrostatic wafer chuck are not yet mounted. Once in operation, the stage will position and scan a wafer within ±3nm of its ideal position.

Figure 9 shows a maglev wafer stage under construction at Sandia, where ETS integration is being performed. Because the maglev stages are essentially friction free, they require very low power actuators and produce virtually no particles that, in the high vacuum of the camera enclosure, could easily damage the reticle or optics.

The maglev stages are controlled by several real-time embedded processors. These processors continuously compare sensor readings to an ideal-position model and attempt to drive the difference to zero through the stage actuators, using complex feedback and control algorithms. The optical bench that mounts the sensors and metrology interferometers for the wafer stage is shown in Figure 10. The ETS goal for the wafer and reticle stages is to track within ±3nm, with a jitter of less than 10nm rms. Testbench experiments predict that the ETS maglev stages will beat those goals by a factor of two.

Photo by Keith Diefendorff

Figure 10. The optical bench for the ETS wafer stage holds the sensors and interferometers used in the feedback loop that controls the wafer position.

The reticle stage, camera optics, wafer stage, and associated metrology instruments all mount in a large environmental chamber designed to minimize particulate and chemical contamination. The large chamber, shown in Figure 11, is divided into three zones: reticle zone (top), optics zone (middle), and wafer zone (bottom). The vacuum in each of the three zones is individually controllable; the seals between zones are designed for optimal protection of the enclosed equipment. The reticle zone provides particle protection for the mask by laminar thermophoretic flow. The optics zone is designed to remove carbon and oxygen contamination from EUV cracking of residual hydrocarbons and to operate at the extremely low pressure required for good EUV transmission. The wafer zone is optimized to prevent outgassing from photoresist chemicals from entering the optics zone.

The ETS, shown in Figure 12, is in the stages of subsystem testing and final integration. The drive laser has been fully operational for more than a year. The illuminator has been assembled, aligned, and tested with a low-power laser. The camera has been aligned with development optics, and the final mirror set is in fabrication. The maglev reticle and wafer stages are nearing completion. Although much work remains, the VNL scientists see no remaining showstoppers to successful ETS operation and say they are on track to print a full wafer with 0.10-micron (100nm) lines and spaces next year.

ETS Is Just a Start

Of course the ETS is not the end of the road. There are many problems to solve and much work to do between ETS and production-worthy EUVL tools. The VNL and EUV LLC members are working to the schedule shown in Figure 13, which calls for first production tools to be delivered in late 2005.

One practical problem facing production EUVL systems is the drive laser. The ETS laser source and associated wavelength refinement and beam delivery equipment are huge—much larger than is desirable for a production cleanroom environment. Synchrotron radiation sources are another candidate, but they are even less compact than lasers. It is also not clear how to extract sufficient power from synchrotron sources to drive a scanning projection-optics system.

The brightest hope for a new source is electric discharge. These sources are small, simple, and potentially inexpensive, but they are less well developed than either laser or synchrotron sources. At high power, there are potential problems with eroded capillary walls and a short source lifetime. But a high-power prototype is currently under development, and progress is being made on solving these problems.

Defect-free mirror and mask production also remains an issue. Although an improvement of a factor of 30,000 has been made in process-added defect reduction over the past four years, an improvement of two more orders of magnitude is still needed. Furthermore, to meet the demands of the production environment, tool manufacturers must build new ion-beam deposition tools.

Some risk remains that reticle defects cannot be controlled during production. Traditional pellicle encapsulation will not work for EUV masks, because the membrane absorbs too much EUV radiation. A scheme involving a removable pellicle and thermophoretic protection during

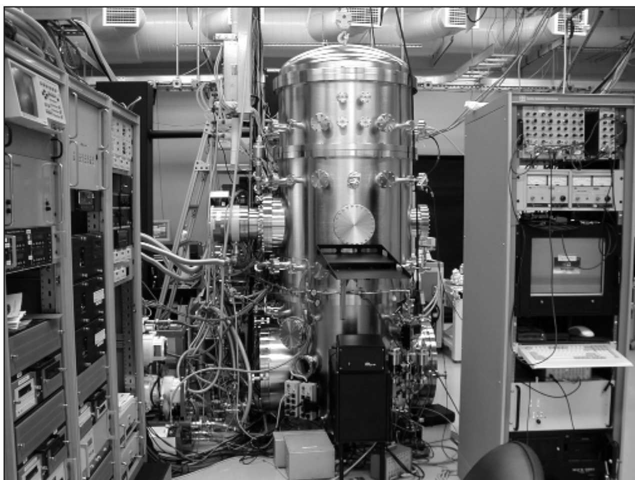

Photo by Keith Diefendorff

Figure 11. Final integration of the ETS camera enclosure. The topmost chamber holds the mask stage; the middle chamber holds the camera optics; and the lower chamber contains the wafer stage. Each chamber is specially designed and individually controlled for optimal protection of the enclosed equipment.

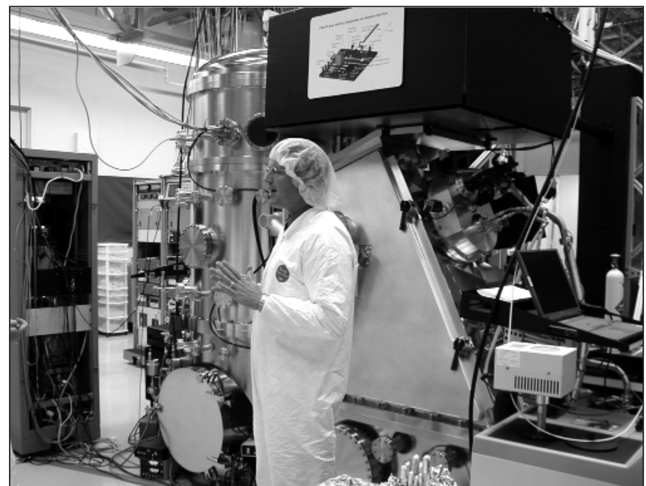

Photo by Keith Diefendorff

Figure 12. This photograph shows the nearly complete ETS. The laser source is several times the size of the ETS itself and is located behind it and to the right, out of the picture. The laser beam enters the illumination chamber from the large black box above it. Xenon gas enters the chamber through the circular access port near the laptop computer. The camera enclosure is behind the illumination chamber and just to the left of it.

exposure has been developed, but the process must still be tested to prove it will be effective.

Mask distortion due to EUV heating during printing is a lurking problem. Although silicon substrates have a sufficiently low coefficient of thermal expansion for use in ETS, substrates made of low-thermal-expansion material will be needed for sub-100nm lithography. Glass substrates of amorphous SiO_2 doped with TiO_2 and special glass-ceramic substrates are under investigation, but work still remains to create surfaces as smooth as those on silicon wafers.

Condenser (C1) lifetime is also still a concern. A 45eV plasma in close proximity to a gas jet can sputter material onto the mirrors, and high temperatures further degrade the coatings. Although the VNL believes its current design will meet requirements, much testing remains to validate this belief. Furthermore, the VNL strategy requires periodic replacement of condenser mirrors, which increases the cost of tool ownership.

Surprisingly, EUV photoresist does not appear to be a significant problem. Acrylic-based resists developed for 193nm lithography are not workable, because their high volatility creates an outgassing problem. Experiments have shown, however, excellent resolution, low line-edge roughness, high sensitivity, low defect rates, and good etch resistance with a single ultrathin layer of 248nm DUV resist over a hardmask. Bilayer resists have also been successfully demonstrated, but they are more complex and costly.

So far, methods for detecting and removing defects down to the limits of optical detection, about 80nm, have been successful. To go further, however, will require more-sensitive inspection equipment. To this end, the VNL is cooperating with KLA-Tencor to develop a DUV-light instrument capable of detecting defects as small as 50nm.

In addition to these critical issues and a host of other engineering issues, there are potentially even more challenging issues surrounding commercialization. While EUV LLC companies have been able to completely fund the effort to bring EUVL to its current state, the VNL says additional funding will be required to make EUV tools production worthy soon enough to keep the industry moving along the Moore's Law curve.

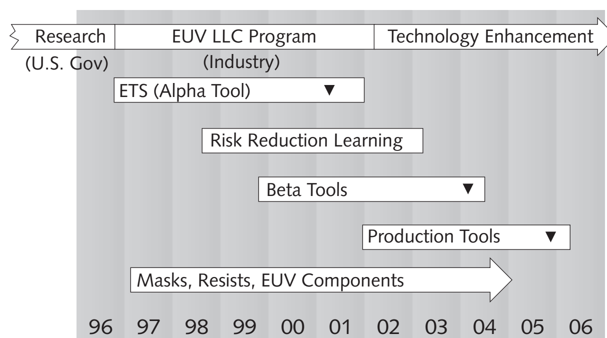

Figure 13. The schedule laid out by the VNL and EUV LLC calls for delivery of production tools to the industry late in 2005, intercepting the industry and Moore's Law at the 70nm generation. (Source: EUV LLC and VNL)

How Much Will it Cost?

Ever since EUVL was first proposed, there has been a hot debate on whether the staggering technical challenges inherent in the technology could be conquered. It is a tribute to the VNL scientists that most of the technical hurdles have been cleared, and the debate these days is shifting to the issue of cost. Depending on the ultimate solutions to the remaining implementation and engineering problems, the capital and operating costs of EUVL equipment could be astronomical.

But the VNL scientists don't believe so. The VNL has been working closely with EUV LLC companies and with semiconductor-equipment manufacturers, such as ASM Lithography, Silicon Valley Group, and US Advanced Lithography, to devise practical solutions to the technical problems. To get a handle on production costs, the VNL has been evaluating its solutions against a cost-of-ownership model supplied by SEMATECH. The model attempts to quantify the cost of each wafer-level exposure.

A major difference between DUV lithography and EUVL is that the laser source and the condenser optics have a shorter lifetime than the stepper has and must be periodically replaced (at considerable expense). Another difference is that EUVL masks must be fabricated with an entirely different process than DUV masks. The economic model takes into account a large number of factors, including stepper costs and depreciation, tool utilization, wafer throughput, mask costs, condenser and laser diode replacement, and resist costs. The most significant factors for EUVL turn out to be capital depreciation and mask costs.

The VNL estimates that a 300mm EUVL stepper will cost approximately $15 million, including vendor markup and installation (a current 200mm 248nm DUV stepper costs $8 million–$10 million). The target cost for an EUV mask is $28,000 (good for 4,000 wafer exposures), although current costs are more like $43,000 (for 2,800 exposures).

The throughput of an EUV stepper is largely a function of the optical flux that makes it through to the wafer. On the basis of the ETS design (27% EUV collection efficiency, seven normal-incidence mirrors, two grazing-incidence mirrors, spectral-purity filter, optics/wafer chamber window), throughput is predicted to be the equivalent of about ten 300mm wafers per hour. With anticipated improvements in mirror reflectivity, source power, resist sensitivity, and wafer setup time, the VNL expects commercial steppers to achieve 80 wafers per hour, which is about that achieved by 248nm DUV steppers.

Considering all these factors, the VNL concludes that EUVL cost of ownership will be approximately the same as that of 157nm steppers using optical proximity correction and phase-shift masks. One important factor not considered

in this study is wafer yield. At the 70nm node, the relaxed k_1 and k_2 values and the greater depth of focus should give EUVL an advantage in process latitude, and thus yield. At 70nm, however, EUVL will be new and probably not as far along the learning curve as 157nm steppers.

Beyond the 70nm node, however, EUVL will have a clear advantage over 157nm steppers, if indeed 157nm steppers get there at all. The current ETS design is limited to 100nm lithography by its relatively small numerical aperture (0.1), but several four-mirror designs have been proposed to increase NA to 0.14, allowing the ETS to perform 70nm lithography. To go below 70nm, however, requires larger NAs. One candidate design is a six-mirror design. With six mirrors, optical throughput is cut in half, but the NA can be increased to 0.25 and the number of degrees of freedom for dealing with aberrations is increased, allowing lithography down to 30nm.

Another option, however, came to light on May 19 when SEMATECH announced it was funding EUV LLC to contract with Carl Zeiss, optics partner of ASM Lithography, to provide advanced EUV optics to the VNL. The VNL will use these optics to create and test a two-mirror high-numerical-aperture camera capable of lithography to 30nm and below. Both the two-mirror and six-mirror designs, because of their higher resolution, have an advantage over four-mirror designs as a first-generation tool. Such a design would eliminate optical-performance variations among the 70nm, 50nm, and 30nm process generations.

To EUVL or to EPL

According to the ITRS99, support for each NGL candidate tends to be regional. EBDW and 1x-proximity XPL are receiving attention in Japan; IPL is being developed in Europe; EPL is popular in the U.S. and in Japan; and EUVL is being developed in all three regions. (The Japanese EUV program is supported within ASET, and the European EUV program is supported within EUCLIDES). The VNL believes that the U.S. EUV LLC program is one to two years ahead of these challengers.

Despite regional preferences, EUVL and EPL clearly have the broadest industry support. The primary hotbeds of EPL activity are at Lucent, with SCALPEL, and at IBM, with PREVAIL (see *MPR 5/1/00-01*, “IBM Paving the Way to 0.10 Micron”). Both EUVL and EPL programs boast significant advances over the past few years, and both approaches have advantages and disadvantages. At this time, a friendly rivalry exists between scientists working on each system, and proponents on both sides freely admit the other alternative has some merits. This contest is likely to become less friendly, however, as both systems approach the commercialization phase and must vie for funds and for the attention of the all-important tool vendors.

On the one hand, EPL systems appear to be somewhat closer to commercial viability than EUVL systems. The ITRS99 calls out EPL as an option for 100nm production by 2003. IBM concurs with this date, and Nikon says it will build a production EPL stepper based on IBM’s PREVAIL system for delivery within that time frame. If the Nikon stepper works well, EPL could save the industry an expensive excursion into 157nm optical steppers, which are doomed to last only a short time. Also, if commercial EPL systems get a three-year head start on EUVL systems, the latter could have a tough time catching up.

EPL also appears to have some benefit in cost of ownership. EPL steppers can generally be somewhat more compact than EUVL steppers, and EPL steppers are likely to have costs closer to, or possibly even less than, today’s DUV steppers. EPL steppers have fewer expensive parts that require periodic replacement, and masks are likely to be less expensive than either EUVL masks or 157nm phase-shift masks.

The most serious problem facing EPL, however, is throughput. Neither EPL nor EUVL systems can attain the magic 80-wafer-per-hour rate with current technology, but EUVL systems may have an advantage on this issue, although experts still disagree on this point. If there is an EUVL throughput advantage, then EPL would be less desirable in low-cost, high-volume manufacturing situations, since throughput is more important to average cost of a wafer exposure than stepper or mask costs.

EUVL has another slight advantage, in that it is somewhat more like optical lithography than EPL is. Since the industry has a great deal of experience and comfort with optical lithography, and since 248nm DUV photoresist technology appears to be directly transferable to EUVL, the transition to EUVL may meet with less resistance. This advantage may not be large, however, as both systems are different from optical tools in several ways—both, for example, require vacuum systems—and EPL has also demonstrated success with single-layer resists.

There is some (remote) possibility that EPL and EUVL could both succeed and possibly even coexist peacefully. EPL could succeed short term, eventually being replaced by EUVL. Or EPL systems could find a lucrative niche in quick-turnaround, low-volume manufacturing, with EUVL dominating the low-cost, high-volume manufacturing segment. We doubt, however, that the industry can really afford to build and support two costly systems as radically different as EUVL and EPL. It is therefore more likely that the industry will eventually settle on one system or the other. Because the outcome is unpredictable at this time, and because of the high risk of putting all one’s eggs in a single basket, we would not be surprised to see IBM and Lucent join EUV LLC even as they continue to champion EPL. Judging from the progress that the VNL is making on EUVL, the cost of this insurance seems justified.

Hats Off to Intel

Although it is too early to jump to the conclusion that EUVL will win the NGL race and become a commercial success, the odds look good. If it does, it will add credibility to the hotly

debated notion that military and space technology can be brought to bear in the private sector with enormous benefits to society—even if the ultimate value of the technology is not always clear at the time of the initial investment.

But regardless of whether EUVL wins or loses, not enough can be said about the accomplishments of the VNL scientists in just a few years. One by one, technical hurdles that once looked insurmountable have been conquered. Superhuman progress has occurred on many fronts: creating clean high-intensity EUV-light sources; producing ultrahigh-precision optics; taming flare at short wavelengths; producing uniform multilayer mirror coatings; controlling thermal stress in a vacuum environment; mitigating defects on optical elements (including reticles); and designing, manufacturing, and controlling mechanical systems to nanometer accuracy.

The technical accomplishments have been impressive, but the real credit for the current status of EUVL must go to Intel. Intel recognized the potential of EUV and realized the national labs might have some technology to bring to bear on the problem. Intel also demonstrated real leadership by setting an example and committing its own money to the effort early on, and then rallying industry support for the technology through lobbying at SEMATECH and by creating EUV LLC. The result is that EUVL technology has gained enormous momentum and come from behind to become the leading candidate for next-generation lithography. Intel and its EUV LLC partners stand to reap the benefits by gaining early access to the billion-transistor chips the technology enables. ◇

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