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TriCore Turns 1.3

By Peter N. Glaskowsky {7/17/00-06}

At last month's **Embedded Processor Forum**, Infineon announced version 1.3 of its TriCore architecture (see *MPR 4/19/99-02*, "Infineon's TriCore Tackles DSP") and described a "V1.3 MicroProcessor System" macro meant to be implemented in a 0.18-micron, five-layer copper-interconnect process along with additional application-specific logic. The design includes a 3mm^2 CPU based on the new core architecture that runs at speeds up to 200MHz. The macro's 32K instruction cache and 32K data cache may each be split into a 16K cache plus a 16K SRAM.

The macro, which has 5.9 million transistors, includes on-chip debug and power-management logic as well as three external interfaces—one for a coprocessor, one for local memory, and one for peripherals. Infineon also designed in a new MMU that supports virtual-memory operating systems such as EPOC32, Linux, and Windows CE.

At the Forum, Infineon also described how to integrate four of these macros on a single die, connected by their peripheral-bus interfaces. Though the small size of the TriCore CPU core makes this plan affordable, software development for such a chip would be more complex than for single-core processors. To simplify the software-development task, the four processors would share a unified address space, and each would have a unique CPU ID.

Infineon expects to begin sampling application-specific standard products (ASSPs) based on the V1.3 core in late 2000. The new core is also available for licensing. More information is available online at *www.infineon.com*.