Literature Watch

Audio/Video

Audio/Video processor fits applications from Palmtop to home theatres. A scalable, modular architecture delivers the performance and flexibility needed to satisfy a wide range of media applications. Dave Bursky, *Electronic Design*, 3/6/00, p. 66, 5 pp.

Buses

Triple-port PCI-to-PCI bridge increases support for system expansion slots. This innovative device enhances overall system performance through concurrent bus communication. Joseph Desposito, *Electronic Design*, 5/29/00, p. 60, 3 pp.

Design Tools

Get a handle on design languages. SOC requirements are forcing the industry to scramble to find a solution to system-design problems in the shortest possible time. Will the effort yield a success story? Gabe Moretti, *EDN Europe*, 6/00, p. 54, 8 pp.

Development Tools

Co-verification and system abstraction levels. System-on-chip designs require development tools and methodologies that enable concurrent design, debug, and verification of hardware and software. This article identifies key attributes of the various system abstraction levels and a methodology that describes how designers use them to work together in a co-verification development environment. Bob Morasse, Intrinsix; *Embedded Systems Programming*, 6/00, p. 90, 9 pp.

DSP

Portable vector math libraries. Vector math libraries are used to perform calculations on arrays. This article compares and contrasts the different vector-processing capabilities that are available in hardware and suggests techniques for making vector libraries more portable. William Wright and James Metzger, BBN Technologies; *Embedded Systems Programming*, 6/00, p. 104, 11 pp.

IC Design

Hierarchical ASIC design at three million gates and above. DSM processes demand implementation of the top-level physical design before performing logic design. Toshio Aizawa, NEC Electronics, and Ravi Thummarukudy, GDA Technologies; *ISD*, 7/00, p. 54, 5 pp.

Emulation technology for ASIC core verification. A comprehensive look at an emulation strategy that was used on three ASIC cores. Alan Singletary, IBM Microelectronics; *ISD*, 7/00, p. 27, 5 pp.

Rdram modeling issues and challenges. Modern processor design teams demand more than a functional model. They also need accurate timing analysis, clock skew and jitter, wire delays, debug hooks, and good simulation performance. Scott Taylor, Compaq, and Nicholas Jamba, Avici Systems; *ISD*, 7/00, p. 44, 5 pp.

Memory

Adding error-correcting circuitry to ASIC memory. Thinking of putting ROM or RAM onto an ASIC? Then consider adding error-correcting code (ECC) circuitry as well. Its presence boosts yield and reduces problems with random single-cell defects in memory arrays. Ken Gray, Philips Semiconductors; *IEEE Spectrum*, 4/00, p. 55, 6 pp.

Serial EEPROMs answer designers' needs for more point storage. Available with a wide variety of interfaces and features, serial EEPROMs deliver nonvolatile memory in sizes from under 1Kbit to 1Mbit. Dave Bursky, *Electronic Design*, 3/6/00, p. 93, 5 pp.

Miscellaneous

Encryption wars: early battles. With the rise of hard-to-crack encryption, sensitive data is easier to protect—and criminal activity tougher to monitor. Michael A. Caloyannides, Mitretek Systems; *IEEE Spectrum*, 4/00, p. 37, 7 pp.

Jini to the rescue. A new approach to creating networks could simplify their construction and adaptation—if some kinks in the current specification can be remedied and missing features added. Steve Morgan, ObjectSpace; *IEEE Spectrum*, 4/00, p. 44, 6 pp.

MEMs designs gear up for greater commercialization. As new markets arise, MEMs and MST technologies move forward to overcome challenging packaging, testing, reliability, and manufacturing roadblocks. Roger Allan, *Electronic Design*, 6/12/00, p. 85, 7 pp.

Predicting semiconductor failure modes. With the growing trend toward miniaturization and the need for portable low-power gadgets operating in all types of stressful environments, designing high-reliability products is becoming a challenging task for electronic product designers. Venkataraman Lakshminarayanan, Centre for Development of Telematics; *ISD*, 7/00, p. 62, 6 pp.

Peripheral Chips

ICs drive down the cost of connectivity for Gigabit Ethernet over copper. An end-to-end solution is expected to bring ultrafast networking right to the desktop. Joseph Desposito, *Electronic Design*, 6/12/00, p. 78, 3 pp.

Processors

Stepping down to 8 bits. At least two factors suggest that moving to a more powerful processor doesn't necessarily mean taking on more bits. As applications mature, powerful, function-specific processors, or engines, become available to take on most of the grunt work. Nicholas Cravotta, *EDN Europe*, 5/00, p. 49, 8 pp.