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# EMBEDDED TIDBITS

*By Mark Long [9/25/00-04]*

## C-CUBE UNVEILS SOC FOR DIGITAL STBS

C-Cube has unveiled a chip for digital set-top box (STB) manufacturers that integrates multiple dedicated processing units, including a host CPU, A/V decoder, audio DSP, and graphics processor. The integrated 150MHz microSPARC CPU can act as host and supports applications like digital time shifting and soft modem.

The AViA-9600 has both IEEE-1394 and USB ports for connecting digital cameras/camcorders, external hard-disk drives, DTVs, and printers to the STB. An IDE controller is also included to provide a direct connection to hard-disk drives to permit time shifting. In addition, the AViA-9600's MPEG decoder is equipped with multiple play modes that will allow STB users to pause, review, and fast-forward video programs stored on a hard disk.

The AViA-9600's A/V decoder is fully compliant with DSS (DirecTV) and the DVB broadcast standard, as well as DVD and DES encryption. The chip offers support for 5C copy protection for the secure distribution of content over IEEE-1394. It also offers CPRM-based (Content Protection for Recordable Media) encryption for copy protection of content stored on hard-disk drives. The AViA-9600's audio DSP can process multiple audio formats, including MPEG-2, Dolby Digital and DTS.

Samples of the AViA-9600 will be available beginning next month, with volume production set to commence in 1Q01. Volume pricing for the AViA-9600 in a 308-BGA package will be less than $22 per unit. For more information: *www.c-cube.com*.

## SILICON SPICE INTROS COM CHIP

Silicon Spice has introduced CALISTO, a single-chip communications processor for carrier-class voice gateways, soft switches, and remote-access concentrators/remote-access servers (RAC/RAS). The new chip, says Silicon Spice, replaces up to 10 traditional DSP discrete components, achieving more than 400 channels/in.$^2$ while consuming less than 10mW per channel.

The CALISTO (for configurable algorithm-adaptive instruction set topology) chip has been designed to manage a variety of DSP and packet-processing tasks, including echo cancellation; voice/fax- and data-modem signal processing; packetization; delay equalization; and telephony protocols within packet-telephony applications. The chip architecture reportedly provides more than 3.3 GMACs of signal-processing horsepower and 1.4MB of high-speed memory, which translates into 240 packet-telephony channels on a single chip.

According to Silicon Spice, CALISTO's RTOS enables voice and data service providers to dynamically provision CALISTO for Any Service Any Port (ASAP) configurations ranging from 240 channels of carrier-class G.711 packet telephony to 60 channels of full Universal Port. Featuring a 239-pin BGA, the CALISTO device is augmented by an IDE that includes an optimizing C compiler and multiprocessor debug environment. Currently sampling, CALISTO will be in full production by the end of the year. For more information: *www.silicon-spice.com*.