PATENT WATCH

By Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@arithmetic.stanford.edu *with comments or questions.*

6,073,185

Parallel data processor

Filed: August 27, 1993 **Issued: June 6, 2000**
Inventor: Woodrow Meeker **Claims: 29**
Assignee: TeraNex

A parallel processor has a controller generating control signals and multiple identical processing cells, each of which is connected to at least one neighbor cell. Each cell includes memory, at least two registers, and an ALU. An input of the first register is coupled to the cell's memory output. The output of the first register is coupled to a register in a neighboring cell. An input of the second register receives an output from a first register located in a neighboring cell. The output of the second register is coupled to an input of the ALU.

6,073,150

Apparatus for directing a parallel processing computing device to form an absolute value of a signed value

Filed: June 23, 1997 **Issued: June 6, 2000**
Inventor: Vladimir Volkonsky **Claims: 3**
Assignee: Sun

A method for computing an absolute value of a signed N-bit value consists of the following steps: arithmetic right shifting an N-bit input value by N-1 bits to form a bit mask; XORing the bit mask and the N-bit value; subtracting the bit-mask from the result of the XOR.

6,070,237

Method for performing population counts on packed data types

Filed: March 4, 1996 **Issued: May 30, 2000**
Inventors: Alexander Peleg et al. **Claims: 13**
Assignee: Intel

A packed data item includes two data elements of predetermined widths. A processor operating on the packed data produces a result packed data item containing two independent data elements. The result elements will contain the total number of bits "set" in each of the corresponding input elements of the packed data item.

6,070,235

Data processing system and method for capturing history buffer data

Filed: July 14, 1997 **Issued: May 30, 2000**
Inventors: Hoichi Cheong et al. **Claims: 23**
Assignee: IBM

A data processor includes logic to ensure that result data stored in an architectural-register "backup" buffer is in correct chronological order and is not incorrectly overwritten, particularly when result data delivery is unexpectedly delayed. The buffer stores result data based on tagged identifiers. One cycle before result data is expected to be available, a target identifier assigned to the instruction producing the data is broadcast on a result bus. If the result data is delayed at a next cycle, a reexecute signal is asserted on the result bus to notify the buffer or architectural register that the data is not ready to be stored. The reexecute signal remains asserted until the result data is available. During the same cycle that the reexecute signal is negated, result data is presented on the result bus.

6,067,616

Branch prediction device with two levels of branch prediction cache

Filed: April 26, 1996 **Issued: May 23, 2000**
Inventors: David Stiles et al. **Claims: 11**
Assignee: AMD

An improved branch prediction cache scheme utilizes a hybrid cache structure. The cache provides two levels of branch information caching. A fully associative first level cache encaches full prediction information for a limited number of branch instructions. The second, direct-mapped cache encaches only partial prediction information, but does so for a much larger number of branch instructions. As each branch instruction is fetched and decoded, its address is used to perform parallel look-ups in the two branch prediction caches.

6,067,615

Reconfigurable processor for executing successive function sequences in a processor operation

Filed: November 9, 1995 **Issued: May 23, 2000**
Inventor: Eric Upton **Claims: 17**
Assignee: TRW

A reconfigurable digital processor with a configurable device. The configurable device dynamically reconfigures configurable gate arrays according to stored library functions. The selection of certain library functions for reconfiguring the gate arrays is based on the function library and the results of the execution of certain previously configured functions.

OTHER ISSUED PATENTS

6,070,238 *Method and apparatus for detecting overlap condition between a storage instruction and previously executed storage reference instruction*