

iDragonTM **mP6**TM **Microprocessor Overview**

The RiSETM mP6TM processor is a sixth generation processor optimized for low-power, high-performance information appliance applications. The innovative RiSETM mP6TM processor is the first superscalar, superpipelined, Pentium[®] MMX* compatible processor featuring 3 integer units, 3-way superscalar MMX technology, and a fully pipelined floating point unit. The innovative circuitry of the RiSETM mP6TM processor maximizes processing per clock cycle while requiring minimal power consumption – providing an ideal choice for power-efficient PC-embedded consumer information appliance, thin server and thin client,



- **x86 Instruction Set Enhanced with MMXTM Technology**
- **Pin Compatible with the Intel Pentium, AMD* K6, AMD K6-2, and Cyrix MII* Processors (Socket 7)**
 - 296 Pin BPGA “Socket 7” Package
 - 387 Ball T²BGA[®] “Socket 7-like” Package
 - Split Voltage Planes
- **Advanced Architectural Features**
 - Advanced Data Dependency Removal Techniques
 - Innovative Instruction Decode and Branch Prediction
 - Dynamic Allocation of Resources
- **Superscalar, Superpipelined Architecture**
 - Superscalar MMX* Execution and Three Superpipelined Integer Units
 - Pipelined Floating Point Unit
- **Separate Code and Data Caches**
 - 8KB Code and 8KB Data
 - Filtered Tag Prefetching
 - Split Line Access Mechanism
- **Advanced Power Management and Power Reduction Features**
 - SMM Compatible
 - Clock Control
 - ACPI Compliant
 - Facility Gating
 - Required Selection Only
 - Necessity Switching Only
- **High Performance FPU**
 - IEEE 854 and 754 Compliant
 - 80 Bit Results, 64 Bit Interface
- **IEEE 1149.1 Boundary Scan**
 - IEEE 854 and 754 Compliant
 - 80 Bit Results, 64 Bit Interface
- **ISO 9001 Wafer Fabrication, Assembly and Test**
- **Support for Bus Frequencies of 60, 66, 75, 83, 95, and 100 MHz**
- **CPU/Host Bus Ratio 2X, 2.5X, 3X, 3.5X**
- **3.3 V/2.0 V CMOS Technology**

Figure *MP6*TM Processor Block Diagram

