LC4 Hardware Description and Installation Manual

Form 157

LC4 HARDWARE DESCRIPTION AND INSTALLATION MANUAL

Form 157-990415 — April, 1999

OPTO 22

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THE LC4 LOCAL CONTROLLER

The LC4 is a powerful, low-cost, single-board computer designed and manufactured by OPTO 22 to perform the function of a local controller on an OPTOMUX intelligent I/O network. The LC4 has been designed to incorporate many features found in personal computers while maintaining the necessary dedication of a local controller. The LC4 features an expansion port for easy customization to special needs.

Basic Architecture

The heart of the LC4 is a 64180 8-bit microprocessor operating at a clock frequency of 6.144 MHz. For memory, the LC4 uses 64 Kilobytes of CMOS Static RAM which is battery backed up for non-volatile storage of user programs and data. To give the LC4 programming power, 64 Kilobytes of Read Only Memory (ROM) contains a BASIC interpreter that is command compatible with Microsoft BASIC or a FORTH interpreter, the interface driver to the OPTOMUX network and the interface driver to the PAMUX network. Two RS422/485 communications ports are provided; one to communicate with a host and another to communicate with the OPTOMUX network. The RS422 standard is preferred over RS232 because of its excellent noise immunity and capability of transmitting over longer line lengths (up to 5000 ft) at higher baud rates. The host RS422\485 channel can be selected to use RS232 levels for compatibility with most terminals and microcomputers. A battery backed up real time clock is also provided for time dependent tasks.

- **Note: This manual is for LC4s marked "Rev A" and above.**
  For LC4s with no revision letter please refer to Form 157.
  Revision A LC4s have "Address" jumpers and no 4TH jumper.

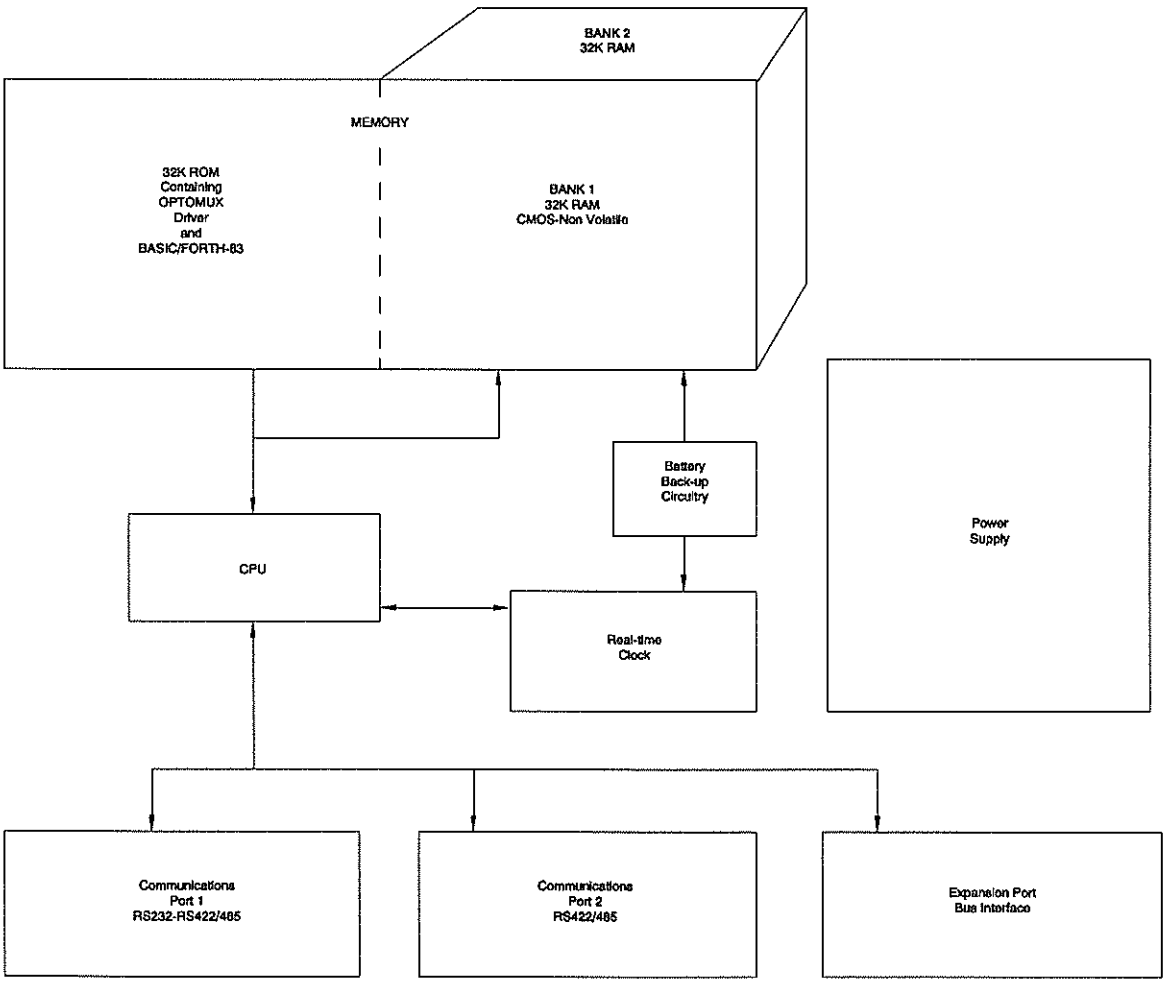


Figure 1 - LC4 Block Diagram

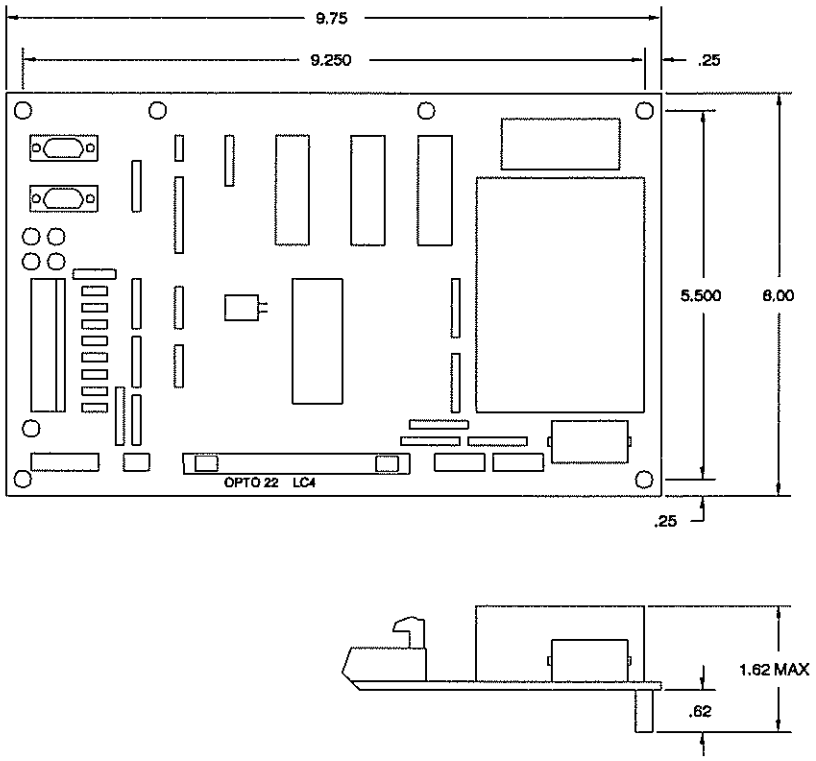


Figure 2 - LC4 Dimensions

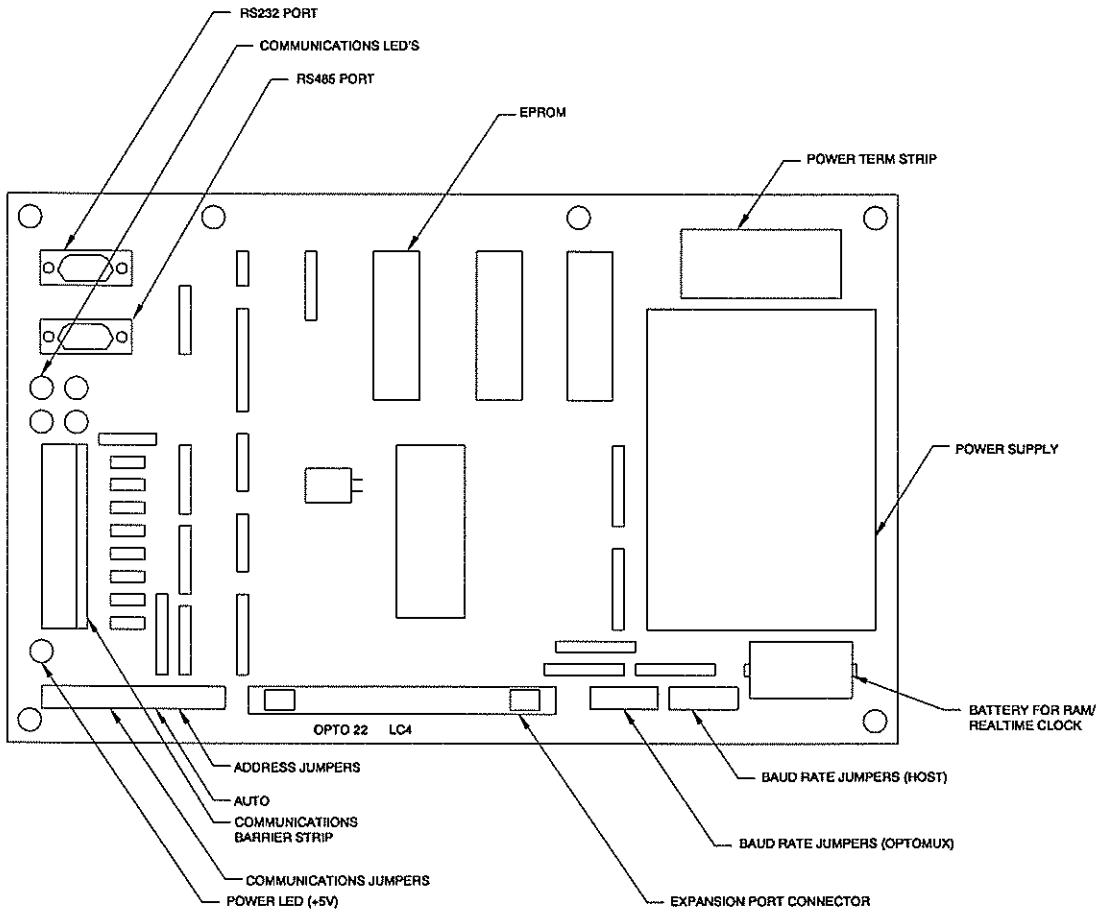


Figure 3 - LC4 Major Components

INSTALLATION AND WIRING

The following steps will describe how to properly configure and install your LC4 local controller.

STEP 1: Communication Cables

All of the communications terminals on the barrier strip are duplicated on the female 9-pin "D" shell connector, labeled RS-485. This gives you a choice as to which type of connection to use. Refer to the wiring diagrams following this section for information on cable connections and pin assignments. The wiring diagrams show host to LC4 cabling using either the female 9-pin "D" shell connector or the terminal barrier strip. If you are using an OPTO 22 RS422 card (Model AC24 or AC422), please note that the wiring is NOT a straight through, pin for pin connection between the two 9-pin "D" shell connectors.

For each port, use a 22-gauge (minimum) cable with two twisted pairs. Connect the wires as shown in the wiring diagrams (Figures 4 & 5).

Double check your wiring after it is complete, then continue with the next step.

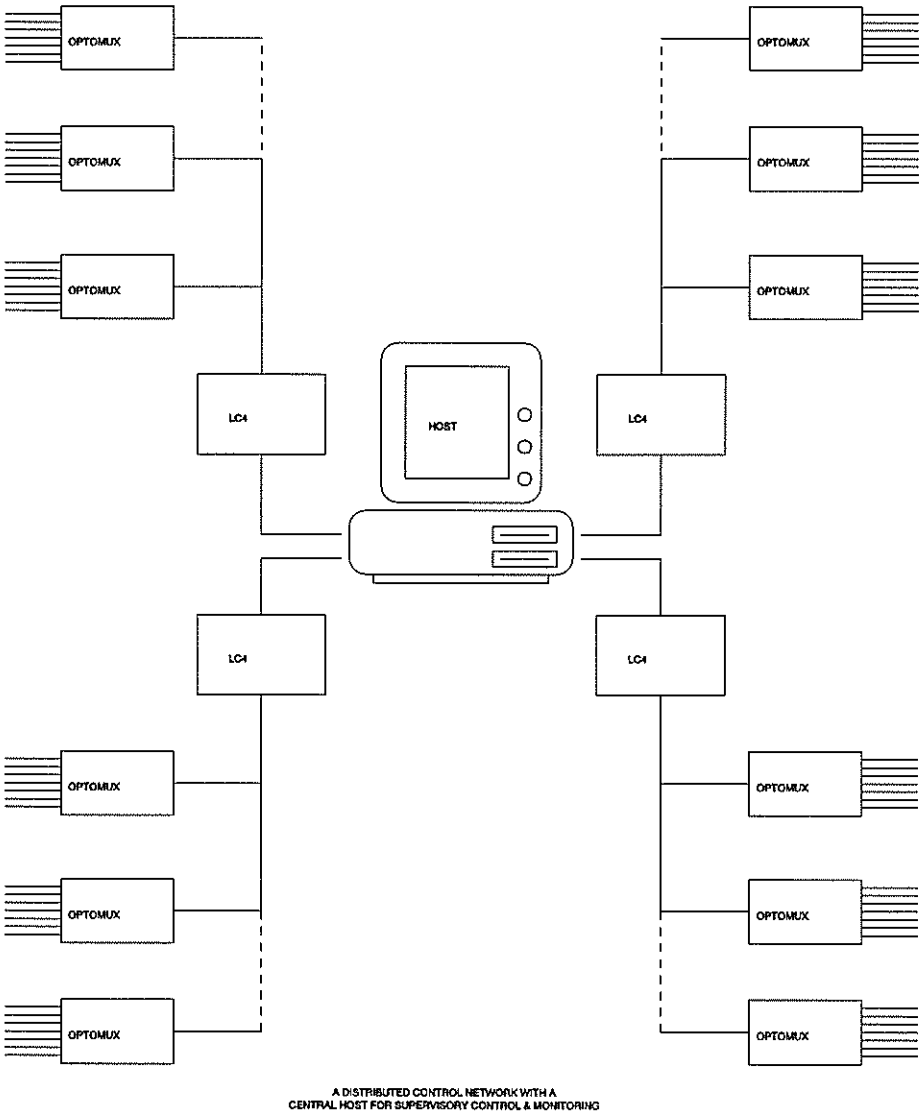


Figure 4 - Wiring Using Terminals

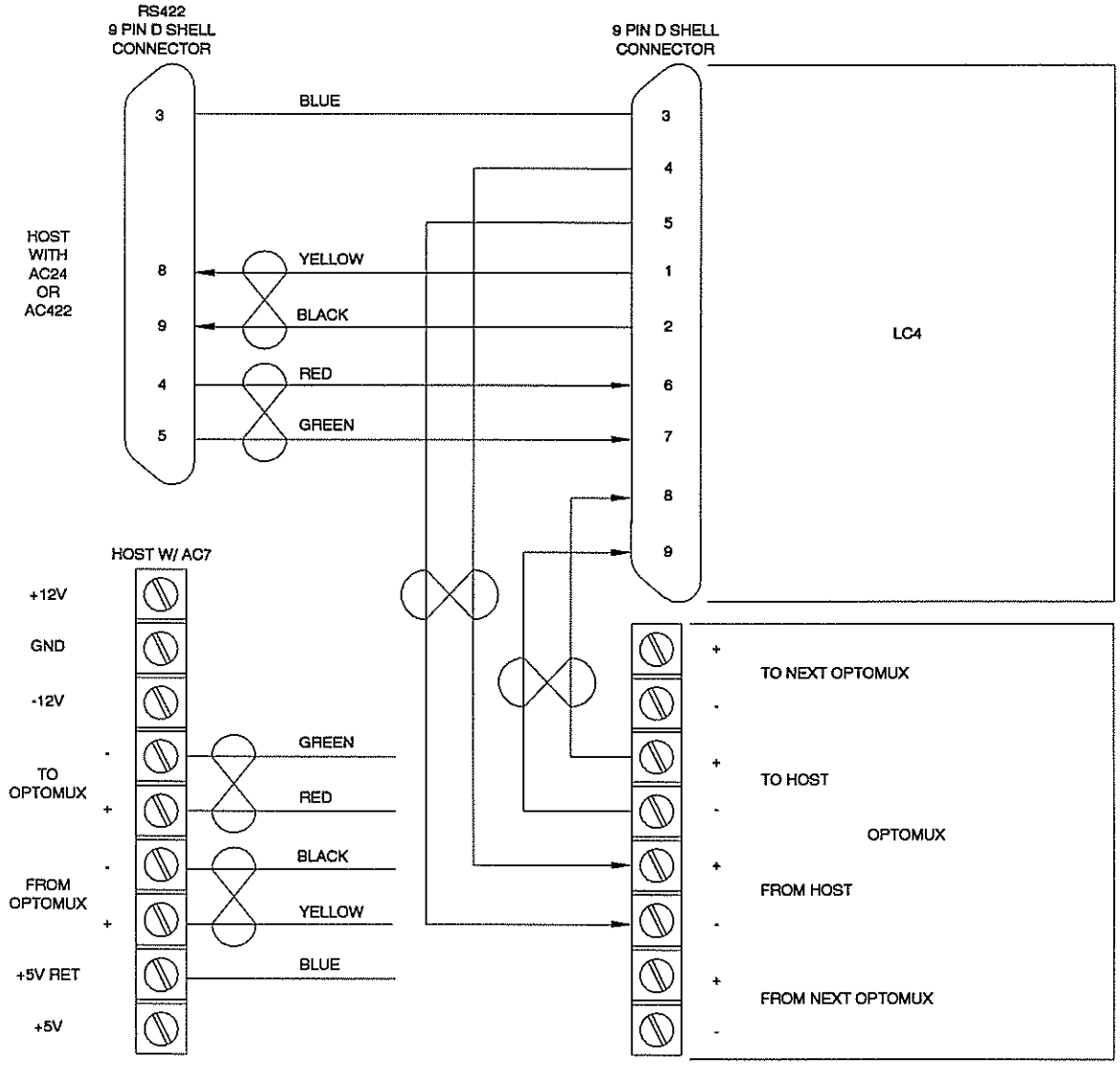


Figure 5 - Wiring Using D-Shell

STEP 2: Setting the Jumpers

There are two groups of jumpers for selecting the baud rate; one group for each communications port. The group of jumpers corresponding to the host port is labeled "Baud Host", the group corresponding to the OPTOMUX port is labeled "Baud Optomux".

The two communication ports are independent of each other. A different baud rate may be specified for each port, but only install one jumper per group.

Install the jumper for the desired baud rate on the group "Baud Host" block for communications with a host device.

Example: By installing the jumper in the position marked 19.2K, the baud rate for the host port is set to 19200 baud.

BAUD HOST

:	:	:	:	:	X	:
300						**38.4K**

X indicates jumper is installed

After installing the jumper for the host port baud rate, install the jumper for the OPTOMUX port (group "Baud Optomux").

INSTALLING THE "COMMUNICATIONS" JUMPERS

The "Communications" jumpers are used to add termination resistors and appropriate pull-up or pull-down resistors to each communication pair.

The following examples illustrate which jumpers should be installed for specific applications. In order to properly balance the communications line, the termination resistors should be installed only on the devices at each end of the link. Only one device on the entire link should have the pull-up and pull- down resistors. Refer to the Communications Jumper Schematic (Figure 6) for a diagram of each jumper and its corresponding resistor.

EXAMPLE 1:

One LC4 connected to a host device (a terminal or computer with an RS422 communications interface).

Communications

1	2	3	4	5	6	7	8
X	X	X	X	X	X	X	X

X indicates jumper is installed

Refer to the operations manual of the communications interface at the host device for configuring the host end.

EXAMPLE 2:

Several LC4s connected in a multidrop configuration (communication lines paralleled).

Devices on each end of the physical link should have termination resistors installed. One device should have the pull-up and pull-down resistors installed (preferably the host).

LC4s on the ends of the link

Communications

1	2	3	4	5	6	7	8
Y	Y	X	X	X	X	X	X

X indicates jumper is installed

Y indicates jumper is installed on only one LC4

LC4s NOT on the ends of the link

Communications

1	2	3	4	5	6	7	8
:	:	X	X	:	X	:	X

X indicates jumper is installed

Installing "Auto" Jumper

Install "Auto" Jumper if you wish LC4 to begin executing the current program in memory on power-up.

Installing "Address" Jumpers

The "Address" jumpers are neccessary only when more than one LC4 is connected in a multidrop configuration on one communications link. In order to communicate to an individual LC4 on such a link, each device must have a unique address. There are eight jumper positions (1 byte) labeled from 0 (LSB) to 7 (MSB) that specify an address between 0 and 255. A jumper installed sets that bit position to a 0, a removed jumper sets that bit position to a 1. All jumpers removed specify an address of 255, All jumpers inserted specify an address of 0.

STEP 3: Configuring the Host and Applying Power to LC4

Refer to the Operations Manual of your host terminal or computer for configuring and initializing the host's serial port. The host should be set up with the following parameters:

BAUD RATE:	300, 1200, 2400 4800, 9600, 19200 or 38400
START BITS:	1
STOP BITS: .	1
DATA BITS: .	8
PARITY: . . .	NONE

If you are using an IBM Personal Computer or compatible as a host, examine the files on the utilities disk provided with LC4. There is a program called LCTERM which will simulate a terminal with upload and download capabilities. The documentation for this program is included in a disk file called LCTERM.TXT.

After the host is configured, apply power to LC4. If everything is working correctly, a sign on message should appear at the host. If this message does not appear, make sure the "AUTO" jumper is NOT installed. If it is installed, turn power off on LC4, remove the jumper, and turn power back on. If you still do not get any response, check the LED indicator "TH" to be sure it flashes briefly when power is applied. This LED indicates that LC4 is transmitting to the host (try a slower baud rate to make it easier to view the flashing LED). Double check the wiring, LC4 configuration, and host configuration to make sure there are no errors.

Every LC4 is tested thoroughly and operated at elevated temperatures for an extended period of time. If after checking the wiring and jumper selections, you are still having difficulty and are in need of further assistance, call our toll-free number (800) 854-8851, weekdays between 8:00 A.M. and 5:00 P.M. Pacific time.

LC4 SPECIFICATIONS

Hardware

CPU: . . . . . Hitachi 64180 8-Bit Microprocessor

CPU CLOCK FREQUENCY: . . 6.144 MHz

EPROM: . . . . . 64 Kilobytes (Intel 27512 or Equivalent)

RAM: . . . . . 64 Kilobytes, CMOS w/Battery Backup

WATCHDOG TIMER: . . . . . Standard, Hardware

REAL TIME CLOCK: . . . . . Clock/Calendar, Epson 62421A, w/Battery Backup

COMMUNICATIONS: . . . . . 2 Full Duplex, RS422/485 Serial Ports
. . . . . Host port also selectable as RS-232

RAM/CLOCK BATTERY: . . . . 3 Volt Lithium, Non-Rechargeable, (RAYOVAC BR-2/3A)

BATTERY LIFE: . . . . . 10+ Years under normal operating conditions

POWER REQUIREMENT: . . . . (At 25 Degrees Centigrade Ambient)
. . . . . LC4A: 115 VAC, 60 Hz, 210 mA max.
. . . . . LC4B: 230 VAC, 50 Hz, 105 mA max.
. . . . . LC4DC: 10-28 VDC, 1.5 Amps @ 10 VDC
. . . . . 0.5 Amps @@@ 24 VDC.

POWER DISSIPATION: . . . . . Less than 7.5 Watts @ 25 Deg. C.

TEMPERATURE: . . . . . 0 to 70 Degrees C. (Operating)

NOTE: Operation at or near maximum rated temperature for extended periods of time may adversely affect reliability.

Software

IBM/PC Command Compatible BASIC Interpreter

FORTH Interpreter (Subset of FORTH-83 Standard with Enhancements)

OPTOWARE - . . . . . OPTOMUX Communications Driver
. . . . . PAMUX Driver

Integer and IEEE Floating Point Arithmetic

Capability to call Assembly Language routines from BASIC

AutoRUN Feature - LC4 will begin executing program on power-up

LC4 JUMPER DESCRIPTIONS

The LC4 Local Controller contains several onboard jumpers which must be configured for proper operation. The jumpers determine the communication baudrates, termination of communication line whether or not LC4 will begin executing a memory resident program on power up and what language will be used. The following table describes each jumper setting:

Communication Jumpers

1 Pull up resistor on "FROM HOST +" line.
2 Pull down resistor on "FROM HOST -" line.
3 Pull up resistor on "FROM OPTOMUX +" line.
4 Pull down resistor on "FROM OPTOMUX -"line.
5 Terminating resistor on "FROM HOST" line.
6 Terminating resistor on "FROM OPTOMUX"line.
7 Terminating resistor on "TO HOST" line.
8 Terminating resistor on "TO OPTOMUX" line.

Jumper in - connects resistor to line

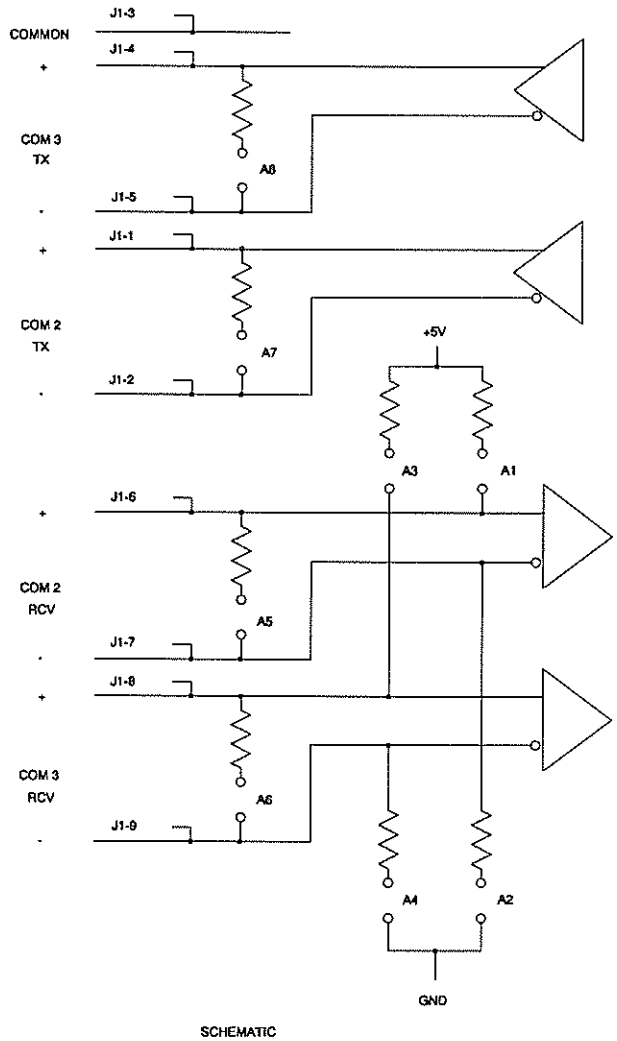


Figure 6 - Communications Jumpers

"Baud Optomux" Jumpers

300	Selects 300 BAUD rate on OPTOMUX comm. port.
1200	Selects 1200 BAUD rate on OPTOMUX comm. port.
2400	Selects 2400 BAUD rate on OPTOMUX comm. port.
4800	Selects 4800 BAUD rate on OPTOMUX comm. port.
9600	Selects 9600 BAUD rate on OPTOMUX comm. port.
19.2K	Selects 19200 BAUD rate on OPTOMUX comm. port.
38.4K	Selects 38400 BAUD rate on OPTOMUX comm. port.

"Baud Host" Jumpers

300	Selects 300 BAUD rate on HOST comm. port.
1200	Selects 1200 BAUD rate on HOST comm. port.
2400	Selects 2400 BAUD rate on HOST comm. port.
4800	Selects 4800 BAUD rate on HOST comm. port.
9600	Selects 9600 BAUD rate on HOST comm. port.
19.2K	Selects 19200 BAUD rate on HOST comm. port.
38.4K	Selects 38400 BAUD rate on HOST comm. port.

On Baud Optomux and Host jumpers, install only one jumper per group for desired BAUD rate.

Auto Jumpers

Installed selects AUTO-BOOT feature. LC4 will automatically begin executing program in memory when power is applied.

Address Jumpers

The "Address" jumpers are neccessary only when more than one LC4 is connected in a multidrop configuration on one communications link. In order to communicate to an individual LC4 on such a link, each device must have a unique address. There are eight jumper positions (1 byte) labeled from 0 (LSB) to 7 (MSB) that specify an address between 0 and 255. A jumper installed sets that bit position to a 0, a removed jumper sets that bit position to a 1. All jumpers removed specify an address of 255, All jumpers inserted specify an address of 0.

The address jumpers are for use with the SLEEP and AWAKE commands for communicating with a single LC4 connected on a multidrop network. The value of the address is stored in the BASIC system variable ADDRESS@ in BASIC and the variable LC.ADDRESS in FORTH. ADDRESS@ and LC.ADDRESS can also be used in communication subroutines within an application program for passing parameters between a host and multiple LC4's.

SPECIAL FEATURES

RS-232

The LC4 is supplied with an RS-232 port offering RTS/CTS handshake capability. This port can be used instead of the RS422/485 Host Port. The RS-232 option is offered for users who do not wish to network the LC4 and want to use the more commonly available RS-232 devices (i.e. terminals, printers...) during programming. The RS-232 connector uses a male nine pin D shell, its pinout is:

- **WARNING: You cannot use an off-the-shelf cable. The following pinouts are the not the standard RS-232 9-pin connector pinouts.**
- **WARNING: If the LC4 is powered off while a device is connected to the RS-232 port, and the device is powered on, battery life will be reduced to less than one year. Any device that is connected to the RS-232 port should either be disconnected from the port or powered off, when the LC4 is powered off.**

Pin	Description
1	No Connection
2	Transmit (TX)
3	Receive (RX)
4	Request-to-Send (RTS)
5	Clear-to-Send (CTS)
6	No Connection
7	Ground (GND)
8	No Connectiong
9	Data Terminal Ready (DTR)

RS-422/485

The RS-422/485 port is wired-OR with the RS-232 port so that two different devices can be permanently connected to the LC4 host communications port. However, it is important to note that only one device can access the port at any one time or characters will be erroneous. This port can be multidropped with up to 100 devices. The RS-422/485 connector uses a female nine pin D shell, its pinout is:

Pin	Description
1	To HOST + (TH+)
2	To HOST - (TH-)
3	Ground (GND)
4	To OPTOMUX + (TO+)
5	To OPTOMUX - (TO-)
6	From HOST + (FH+)
7	From HOST - (FH-)
8	From OPTOMUX + (FO+)
9	From OPTOMUX - (FO-)

Option Port

The LC4 is supplied with a 50-pin, male connector which is designed to allow easy connection of 'Daughter' option cards to the computer bus. OPTO 22 supplies option cards for interfacing to the PAMUX bus and to provide additional peripheral ports.

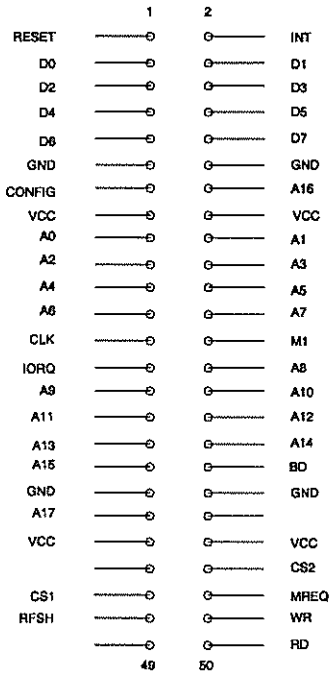


Figure 7 - Option Port Pinout

Notes:

1. BD is pulled low by expansion cards to signal "Board Present"
2. CONFIG is driven low by LC4 to request expansion board type number
   . . . . 1 = PAMUX Adapter
   . . . . 2 = Serial/Parallel
3. CLK is at 6.144 MHz
4. CS1 and CS2 are low active decoded chip selects
5. INT is connected to INT0 on 64180 CPU
6. M1 is not the same as Z80 M1
7. CS1 chip select automatically injects a 2 microsecond wait-state

Option cards currently available include:

EX-1: PAMUX Bus interface card.

EX-2: Serial/Parallel expansion card containing :
1 RS-232 or RS-422/485 serial port
1 RS-422/485 serial port
1 24-bit bidirectional parallel port

MEMORY AND I/O MAPS

Memory Map

The following table shows the layout of the memory banks. The EPROM socket on the LC4 accepts either a 27256 (32K Bytes) or a 27512 (64K Bytes) type EPROM device. If a 32K device is used, disregard EPROM Bank 2.

Location (Hex)	Description
00000-07FFF	EPROM Bank 1 (32K)
08000-0FFFF	EPROM Bank 2 (32K)
10000-17FFF	Program RAM (32K)
18000-1FFFF	Data RAM/RAM Disk (32K)
380E0-380EF	Reserved-OUTCS

I/O Map

The following table shows which locations are used in the I/O space. Locations are shown for the LC4 and the EX-1, EX-2 daughter cards.

Location (Hex)	Description LC4	EX1	EX2
50-5F	RTC		
70-7F	CS-2		DART (70-73)
80-BF	CS-1	PAMUX (80-BF)	PIA 1 (80-83)
			PIA 2 (88-*B)
C0-CF	CONFIG		
D0-DF	INCS		
E0-EF	Hardware Address		
F0-F7		PAMUX RESET	

APPENDIX

Pamux Bus Daughter Card - Model EX1

Description

The EX1 provides a PAMUX bus interface for the LC4. The EX1 can drive up to 512 discrete, or 512 analog I/O points or combinations thereof over a total distance of 500 feet. The EX1 directly maps the PAMUX I/O points into the LC4 processor I/O space. These I/O locations are from 80 Hex to BF Hex. The PAMUX RESET register is at I/O location F0 Hex. For information on using the EX1 adapter card, please refer to the PAMUX Driver Manual and the LC4 Hardware Description and Installation Manual.

The EX1 connects to the LC4's OPTION PORT labeled J3 on the LC4. Connection to the PAMUX bus is performed by connecting a 50 conductor ribbon cable with a male header connector to the female connector labeled J1 on the EX1 card.

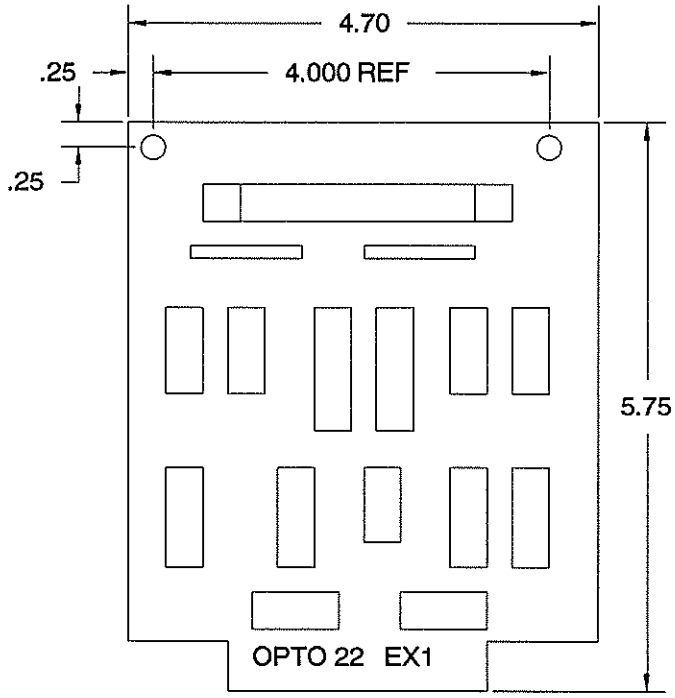


Figure 8 - EX1 Dimensions

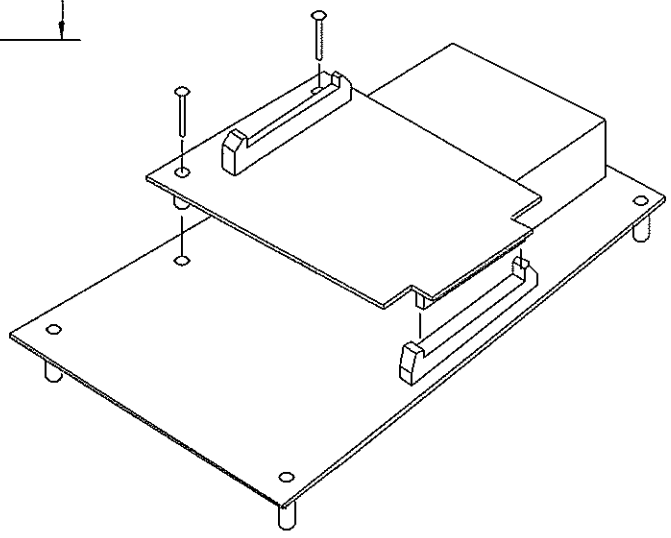


Figure 9 - EX1 Mounting

Serial/Parallel Daughter Card - Model EX2

Description

The EX2 daughter card is an expansion card for the LC4. The EX2 provides two independent full duplex serial communications ports and a 24 line bidirectional parallel port. The parallel port provides a direct interface to 4, 8, 16 and 24 point I/O module mounting racks. One communication port can be RS-232 with full handshaking or a multidrop compatible RS-422/485 port. The second port is RS-422/485 compatible only.

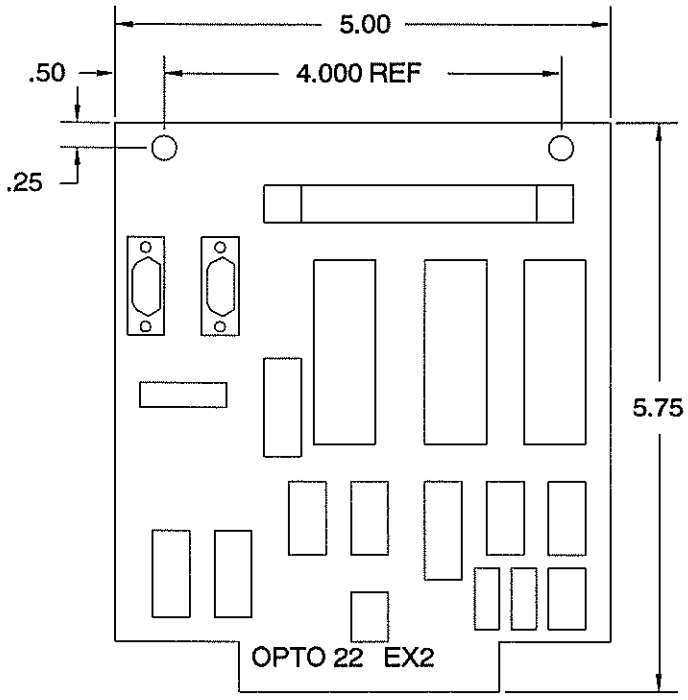


Figure 10 - EX2 Dimensions

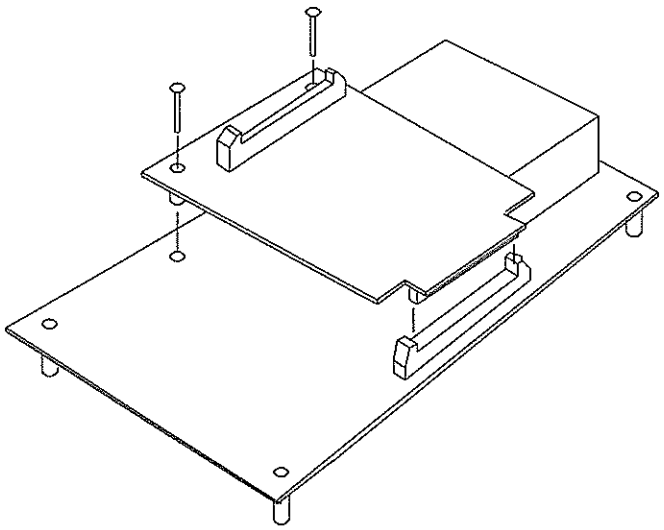


Figure 11 - EX2 Mounting

Serial Ports

The communications ports use a Z80 Dual Asynchronous Receiver Transmitter (DART) device which is directly accessible from LC4 BASIC and FORTH. The DART registers reside at I/O locations 70 to 73 Hex. Baud rates for each serial port are selectable via jumpers labeled "BAUD". The serial ports are labeled as COM 2 for the combination RS-232/RS-422/485 port and COM 3 for the RS/485 port. The RS-422/485 lines of both ports are accessible from the female 9 pin D shell connector labeled J3 on the EX2 daughter card. The RS-232 lines are accessible from the male 9 pin D shell connector labeled J4 on the EX2 daughter card. For more detailed information on the Z80-DART, a data sheet is included at the end of this section.

LED Indicators are provided for the transmit and receive lines of both serial ports. The RS-232 lines are wired-OR with the RS-422/485 lines on the COM 2 port so that two different devices can be permanently connected together. However it is important to note that only one device can access the port at any one time or characters will be erroneous.

A jumper block labeled "GROUP A" provides termination and bias resistor connections for both RS-422/485 ports.

RS-232 Connector Pin Descriptions:

Pin	Description
1	No Connection
2	Transmit (TX)
3	Receive (RX)
4	Request-To-Send (RTS)
5	Clear-To-Send (CTS)
6	No Connection
7	Ground (GND)
8	No Connection
9	Data Terminal Ready (DTR)

RS-422/485 Connector Pin Descriptions:

Pin	Description
1	COM 2 Transmit + (2TX+)
2	COM 2 Transmit - (2TX-)
3	Ground (GND)
4	COM 3 Transmit + (3TX+)
5	COM 3 Transmit - (3TX-)
6	COM 2 Receive + (2RX+)
7	COM 2 Receive - (2RX-)
8	COM 3 Receive + (3RX+)
9	COM 3 Receive - (3RX-)

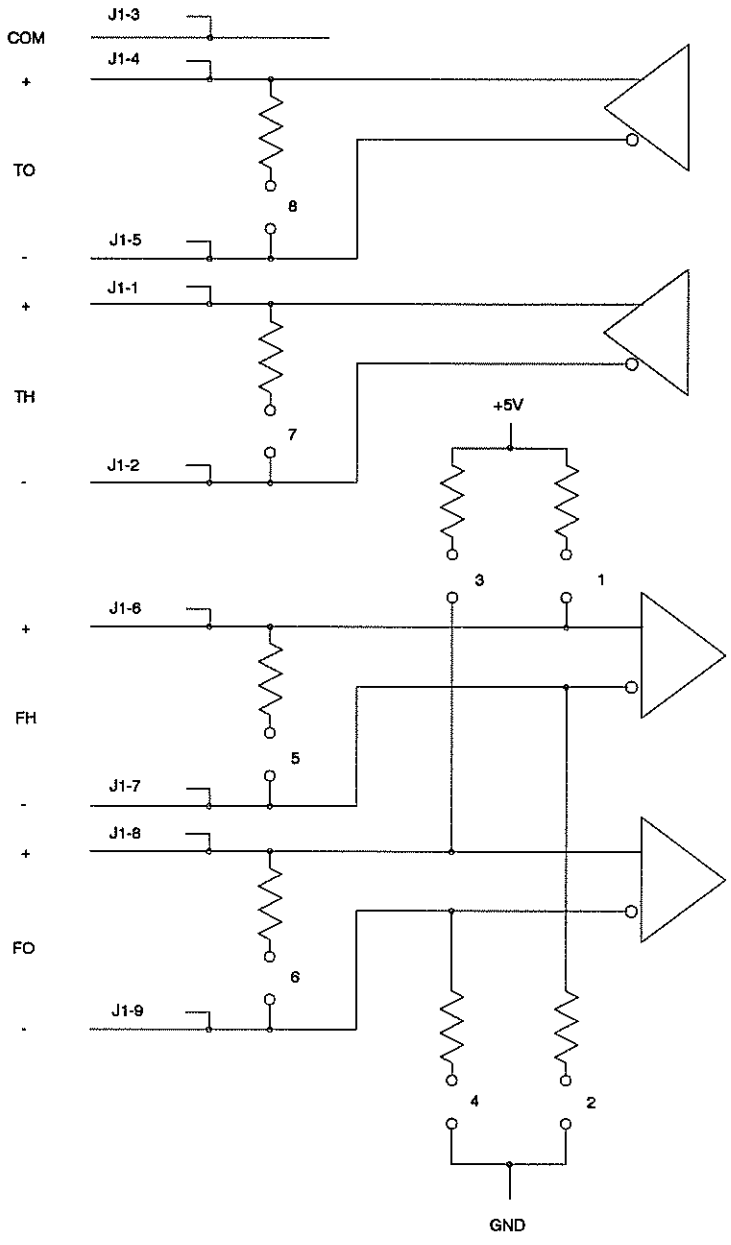


Figure 12 - Group A Communications Jumpers

Parallel Port

The parallel interface consists of two 6821 Peripheral Interface Adapter (PIA) chips which provide a total of 24 lines of un-buffered bidirectional I/O lines. The registers of the PIA for the lower 16 lines resides at I/O locations 80 to 83 Hex. The registers of the PIA for the upper 8 I/O lines (port A of 6821) resides at I/O locations 88 to 8B Hex. The second PIA's port B is not connected. The parallel lines are accessed via connector J2 on the EX2 daughter card. Ports CA and CB on both PIA's are also unused. A data sheet containing more detailed information on the 6821 PIA is included at the end of this section.

Parallel Port Pin Descriptions:

Pin	Description
J2-1	PIA2-A7
J2-3	PIA2-A6
J2-5	PIA2-A5
J2-7	PIA2-A4
J2-9	PIA2-A3
J2-11	PIA2-A2
J2-13	PIA2-A1
J2-15	PIA2-A0
J2-17	PIA1-B7
J2-19	PIA1-B6
J2-21	PIA1-B5
J2-23	PIA1-B4
J2-25	PIA1-B3
J2-27	PIA1-B2
J2-29	PIA1-B1
J2-31	PIA1-B0
J2-33	PIA1-A7
J2-35	PIA1-A6
J2-37	PIA1-A5
J2-39	PIA1-A4
J2-41	PIA1-A3
J2-43	PIA1-A2
J2-45	PIA1-A1
J2-47	PIA1-A0

Notes: PIA1 is at I/O address 80-83 Hex.
PIA2 is at I/O address 88-8B Hex.
All even numbered pins on J2 are connected to ground.

Programming

Parallel Port

There are 8 I/O locations used by both PIA devices. These locations are shown in the following table:

ADDRESS	REGISTER	I/O LINES
80 Hex	Data Reg. A	J2-47 to J2-33
81 Hex	Control Reg. A	
82 Hex	Data Reg. B	J2-31 to J2-17
83 Hex	Control Reg. B	
88 Hex	Data Reg. A	J2-15 to J2-1
89 Hex	Control Reg. A	
8A Hex	Unused	
8B Hex	Unused	

Programming the PIA devices requires that the devices first be initialized. Each I/O line is configurable as an input line or an output line and therefore a configuration byte must be written to each port. The following steps show the sequence of operations for initializing a port.

1. Write a 0 to the corresponding control register.

2. Write the configuration byte to the data register (setting a bit to 1, sets the corresponding I/O line to an output. Setting a bit to 0, sets that I/O line to an input.)

3. Write a hex 34 to the control register.

Example

The following BASIC example initializes the I/O lines at J2-47, J2-45 as outputs and lines J2-43 through J2-33 as inputs. Remember, the PIA devices are I/O mapped and require the use of the OUT and
INP( ) statements in BASIC. (or the P! and P@ words in FORTH).

```
100 OUT &h81,0                  'set control reg. A
110 OUT &h80,3                  'first two bits = 1, rest = 0
120 OUT &h81,&h34               'reset control reg. A
```

After initialization, data can be read or written by accessing that port's data register. The following example reads the status of the input lines J2-47 through J2-33.

```
200 STATUS% = INP(&h80) AND &h03     'read and mask off first two bits
```

The following example shows how to activate I/O lines J2-47 and J2-45 and leave all others off.

```
300 OUT &h80,&hFC                'Turn on first two bits
```

Serial Ports

The 2 serial ports on the EX2 daughter card can be accessed using the BASIC statements OPEN, ON COM..., PRINT #, and INPUT #. Please refer to the LC2/LC4 BASIC Supplement 2.0 for information on these commands.

MOTOROLA

MC6821

MOS
(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

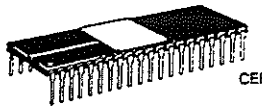
PERIPHERAL INTERFACE ADAPTER

PERIPHERAL INTERFACE ADAPTER (PIA)

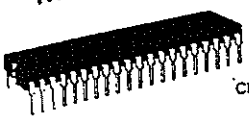
The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the M6800 family of microprocessors. This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functinal configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

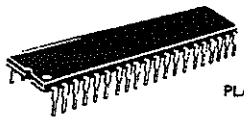
- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-bit Buses for Interface to Peripherals
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation



L SUFFIX
CERAMIC PACKAGE
CASE 715



S SUFFIX
CERDIP PACKAGE
CASE 734



P SUFFIX
PLASTIC PACKAGE
CASE 711

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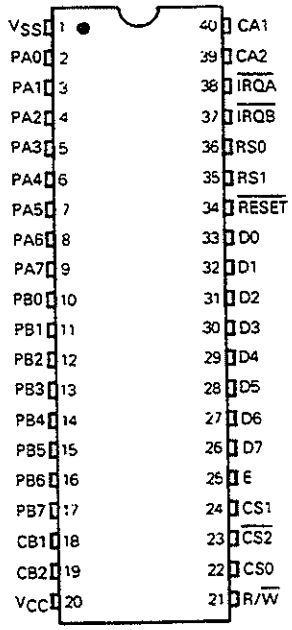
ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic L Suffix	1.0	0°C to 70°C	MC6821L
	1.0	−40°C to 85°C	MC6821CL
	1.5	0°C to 70°C	MC68A21L
	1.5	−40°C to 85°C	MC68A21CL
	2.0	0°C to 70°C	MC68B21L
Cerdip S Suffix	1.0	0°C to 70°C	MC6821S
	1.0	−40°C to 85°C	MC6821CS
	1.5	0°C to 70°C	MC68A21S
	1.5	−40°C to 85°C	MC68A21CS
	2.0	0°C to 70°C	MC68B21S
Plastic P Suffix	1.0	0°C to 70°C	MC6821P
	1.0	−40°C to 85°C	MC6821CP
	1.5	0°C to 70°C	MC68A21P
	1.5	−40°C to 85°C	MC68A21CP
	2.0	0°C to 70°C	MC68B21P

PIN ASSIGNMENT



MC6821

MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6821, MC68A21, MC68B21 MC6821C, MC68A21C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic Cerdip	θ_{JA}	 50 100 60	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $GND \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

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POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} << P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part, K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, $T_A = T_L$ to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BUS CONTROL INPTUS (R/$\overline{W}$, Enable, $\overline{RESET}$, RS0, RS1, CS0, CS1, CS2)					
Input High Voltage	V_{IH}	V_{SS}+2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}−0.3	—	V_{SS}+0.8	V
Input Leakage Current (V_{in}=0 to 5.25V	I_{in}	—	1.0	2.5	μA
Capacitance (V_{in}=0, T_A=25°C, f=1.0 MHz)	C_{in}	—	—	7.5	pF
INTERRUPT OUTPUTS ($\overline{IRQA}$, $\overline{IRQB}$)					
Output Low Voltage (I_{Load}=1.6 mA)	V_{OL}	—	—	V_{SS}+0.4	V
Hi-Z Output Leakage Current	I_{OZ}	—	1.0	1.0	μA
Capacitance (V_{in}=0, T_A=25°C, f=1.0 MHz)	C_{out}	—	—	5.0	pF
DATA BUS (D0–D7)					
Input High Voltage	V_{IH}	V_{SS}+2.0	—	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}−0.3	—	V_{SS}+0.8	V
Hi-Z Input Leakage Current (V_{in}=0.4 to 2.4V)	I_{IZ}	—	2.0	10	μA
Output High Voltage (I_{Load}=−205 μA)	V_{OH}	V_{SS}+2.4	—	—	V
Output Low Voltage (I_{Load}=1.6 mA)	V_{OL}	—	—	V_{SS}+0.4	V
Capacitance (V_{in}=0, T_A=25°C, f=1.0 MHz)	C_{in}	—	—	12.5	pF

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DC ELECTRICAL CHARACTERISTICS (Continued)

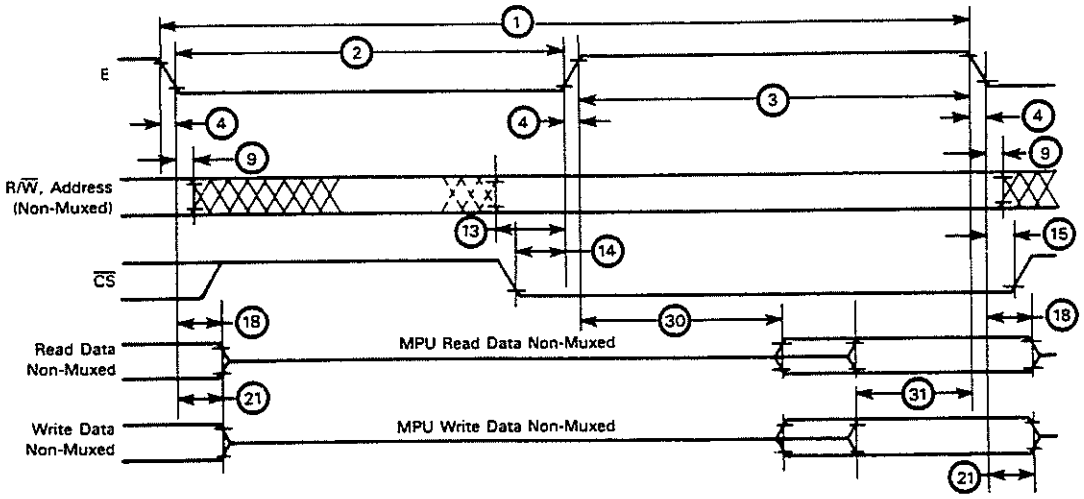
Characteristic		Symbol	Min	Typ	Max	Unit
PERIPHERAL BUS (PA0–PA7, PB0–PB7, CA1, CA2, CB1, CB2)						
Input Leakage Current (V_{in} = 0 to 5.25V)	R/$\overline{W}$, $\overline{RESET}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable	I_{in}	–	1.0	2.5	μA
Hi-Z Input Leakage Current (V_{in} =	PB0–PB7, CB2	I_{IZ}	–	2.0	10	μA
Input High Current (V_{IH} = 2.4V)	PA0–PA7, CA2	I_{IH}	–200	–400	–	μA
Darlington Drive Current (V_O = 1.5V)	PB0–PB7, CB2	I_{OH}	–1.0	–	–10	mA
Input Low Current (V_{IL} = 0.4V	PA0–PA7, CA2	I_{IL}	–	–1.3	–2.4	mA
Output High Voltage (I_{Load} = –200 μA)	PA0–PA7, PB0–PB7, CA2, CB2	V_{OH}	V_{SS} + 2.4	–	–	V
(I_{Load} = –10 μA)	PA0–PA7, CA2		V_{CC} – 1.0	–	–	
Output Low Voltage (I_{Load} = 3.2 mA		V_{OL}	–	–	V_{SS} + 0.4	V
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)		C_{in}	–	–	10	pF
POWER REQUIREMENTS						
Internal Power Dissipation (Measured at T_L = 0°C)		P_{INT}	–	–	550	mW

BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident. Number	Characteristic	Symbol	MC6821		MC68A21		MC68B21		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10	0.67	10	0.5	10	μs
2	Pulse Width, E Low	PW_{EL}	430	–	280	–	210	–	ns
3	Pulse Width, E High	PW_{EH}	450	–	280	–	220	–	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time	t_{AH}	10	–	10	–	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	Chip Select Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	Chip Select Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Output Data Delay Time	t_{DDR}	–	290	–	180	–	150	ns
31	Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

* The data bus output buffers are no longer sourcing or sinking current by t_{DHR}max (High Impedance).

FIGURE 1 – BUS TIMING



Note:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

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PERIPHERAL TIMING (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise specified)

Characteristic	Symbol	MC6821 Min	MC6821 Max	MC68A21 Min	MC68A21 Max	MC68B21 Min	MC68B21 Max	Unit	Reference Fig. No.
Data Setup Time	tPDS	200	–	135	–	100	–	ns	6
Data Hold Time	tPDH	0	–	0	–	0	–	ns	6
Delay Time, Enable Negative Transition to CA2 Negative Transition	tCA2	–	1.0	–	0.670	–	0.500	µs	3, 7, 8
Delay Time, Enable Negative Transition to CA2 Positive Transition	tRS1	–	1.0	–	0.670	–	0.500	µs	3, 7
Rise and Fall Times for CA1 and CA2 Input Signals	t_r, t_f	–	1.0	–	1.0	–	1.0	µs	8
Delay Time from CA1 Active Transition to CA2 Positive Transition	tRS2	–	2.0	–	1.35	–	0.5	µs	3, 8
Delay Time, Enable Negative Transition to Data Valid	tPDW	–	1.0	–	0.670	–	0.5	µs	3, 9, 10
Delay Time, Enable Negative Transition to CMOS Data Valid PA0-PA7, CA2	tCMOS	–	2.0	–	1.35	–	1.0	µs	4, 9
Delay Time, Enable Positive Transition to CB2 Negative Transition	tCB2	–	1.0	–	0.670	–	0.5	µs	3, 11, 12
Delay Time, Data Valid to CB2 Negative Transition	tDC	20	–	20	–	20	–	ns	3, 10
Delay Time, Enable Positive Transition to CB2 Positive Transition	tRS1	–	1.0	–	0.670	–	0.5	µs	3, 11
Control Output Pulse Width, CA2/CB2	PWCT	500	–	375	–	250	–	ns	3, 11
Rise and Fall Time for CB1 and CB2 Input Signals	t_r, t_f	–	1.0	–	1.0	–	1.0	µ	12
Delay Time, CB1 Active Transition to CB2 Positive Transition	tRS2	–	2.0	–	1.35	–	1.0	µs	3, 12
Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$	tCIR	–	1.60	–	1.10	–	0.85	µs	5, 14
Interrupt Response Time	tRS3	–	1.0	–	1.0	–	1.0	µs	5, 13
Interrupt Input Pulse Time	PWI	500	–	500	–	500	–	ns	13
$\overline{RESET}$ Low Time*	tRL	1.0	–	0.66	–	0.5	–	µs	15

* The $\overline{RESET}$ line must be high a minimum of 1.0 µs before addressing the PIA.

FIGURE 2 — BUS TIMING TEST LOADS

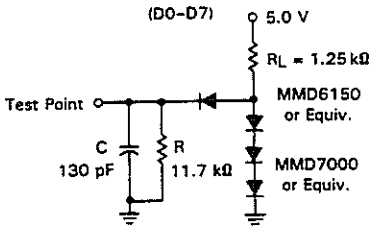
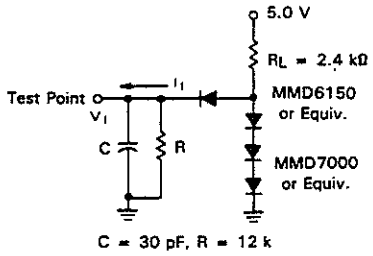


FIGURE 3 — TTL EQUIVALENT TEST LOAD

(PA0–PA7, PB0–PB7, CA2, CB2)



C = 30 pF, R = 12 k

FIGURE 4 — CMOS EQUIVALENT TEST LOAD

(PA0–PA7, CA2)

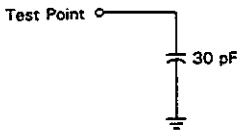


FIGURE 5 — NMOS EQUIVALENT TEST LOAD

($\overline{IRQ}$ Only)

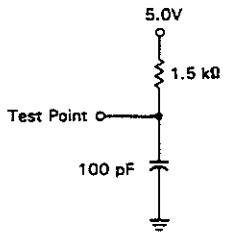


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FIGURE 6 — PERIPHERAL DATA SETUP AND HOLD TIMES
(Read Mode)

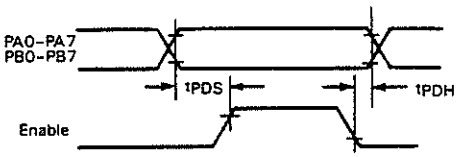
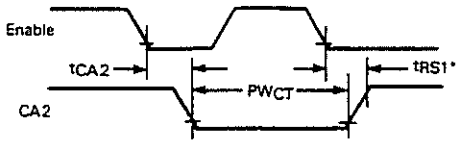


FIGURE 7 — CA2 DELAY TIME
(Read Mode; CRA-5 = CRA3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 8 — CA2 DELAY TIME
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

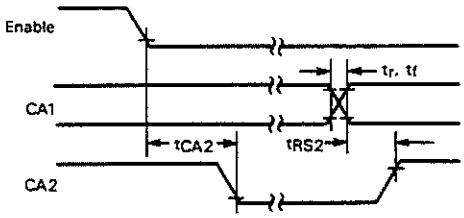


FIGURE 9 — PERIPHERAL CMOS DATA DELAY TIMES
(Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

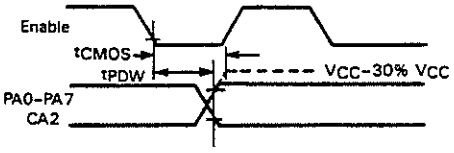
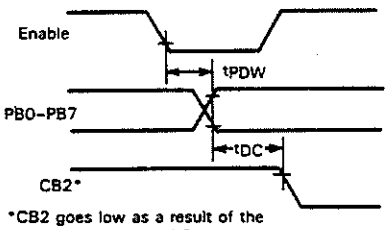
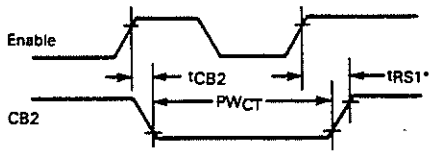


FIGURE 10 — PERIPHERAL DATA AND CB2 DELAY TIMES
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



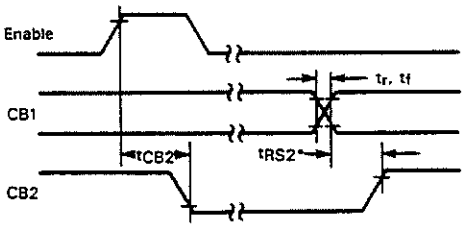
*CB2 goes low as a result of the positive transition of Enable.

FIGURE 11 — CB2 DELAY TIME
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



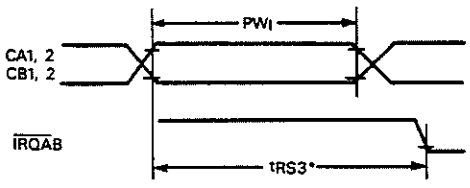
*Assumes part was deselected during the previous E pulse.

FIGURE 12 — CB2 DELAY TIME
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during the previous E pulse.

FIGURE 13 — INTERRUPT PULSE WIDTH AND $\overline{IRQ}$ RESPONSE



*Assumes Interrupt Enable Bits are set.

Note: Timing mesurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

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FIGURE 14 — $\overline{IRQ}$ RELEASE TIME

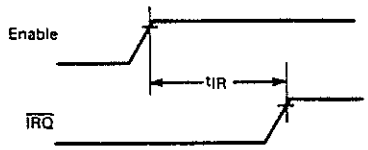
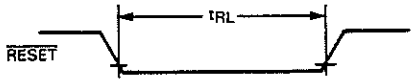


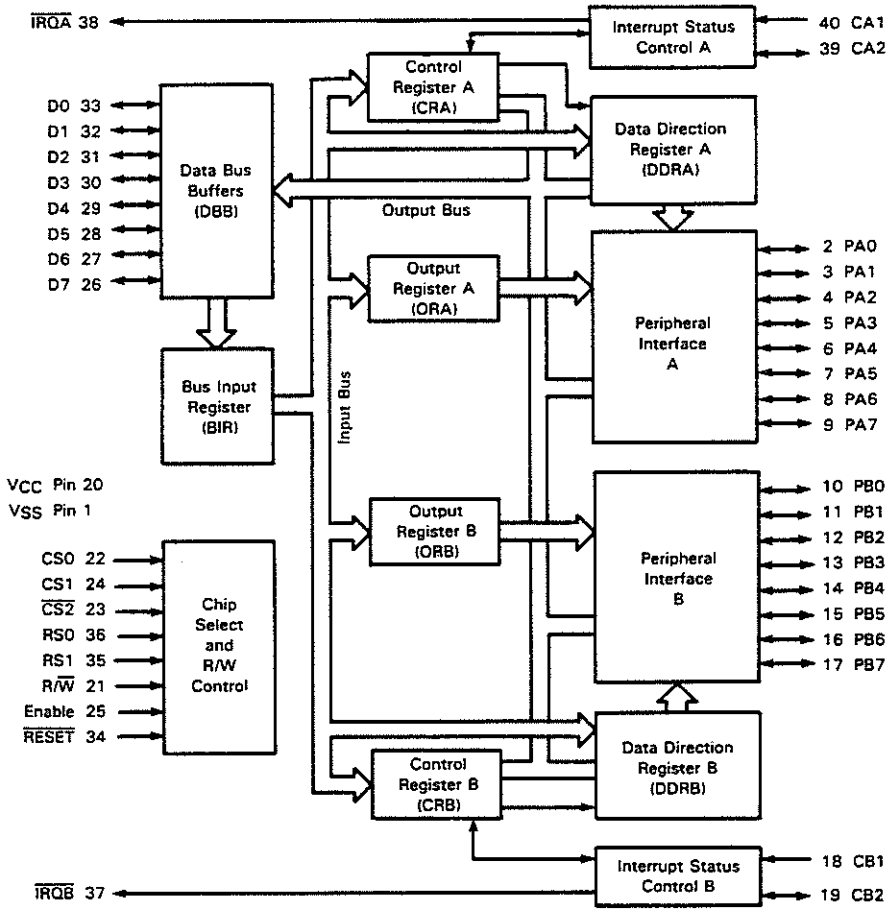
FIGURE 15 — $\overline{RESET}$ LOW TIME



*The $\overline{RESET}$ line must be a V_{IH} for a minumum of 1.0 μs before addressing the PIA.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 16 — EXPANDED BLOCK DIAGRAM



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PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the M6800 bus with an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, a read/write line, an enable line and a reset line. To ensure proper operation with the MC6800, MC6802, or MC6808 microprocessors, VMA should be used as an active part of the address decoding.

Bidirectional Data (D0–D7) — The bidirectional data lines (D0–D7) allow the transfer of data betwen the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The read/write line is in the read (high) state when the PIA is selected for a read operation.

Enable (E) — The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse.

Read/Write (R/$\overline{W}$) — This signal is generated by the MPU to control the direction of data transfers on the data bus. A low state on the PIA read/write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the read/write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

$\overline{RESET}$ — The active low $\overline{RESET}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

Chip Selects (CS0, CS1 and $\overline{CS2}$) — These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{CS2}$ must be low for selection of the device. Data transfers are then performed under the control of the enable and read/write signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

Register Selects (RS0 and RS1) — The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

Interrupt Request ($\overline{IRQA}$ and $\overline{IRQB}$) — The active low Interrupt Request lines ($\overline{IRAQ}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bidirectional data buses and four interrupt/control lines for interfacing to peripheral devices.

Section A Peripheral Data (PA0–PA7) — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low." Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

Section B Peripheral Data (PB0–PB7) — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0–PA7. They have three-state capability, allowing them to enter a high-impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines

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PB0–PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high" or above 0.8V for a "low." As outputs, these lines are compatible with standard TTL and may also be used as a source of at least 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

Interrupt Input (CA1 and CB1) — Peripheral input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

Peripheral Control (CA2) — The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents 1.5 standard TTL loads. The function of this signal line is programmed with Control Register A.

Peripheral Control (CB2) — Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

3

INTERNAL CONTROLS

INITIALIZATION

A $\overline{\text{RESET}}$ has the effect of zeroing all PIA registers. This will set PA0–PA7, PB0–PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

Details of possible configurations of the Data Direction and Control Register are as follows:

TABLE 1 — INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral RegisterA
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

PORT A-B HARDWARE CHARACTERISTICS

As shown in Figure 17, the MC6821 has a pair of I/O ports whose characteristics differ greatly. The A side is designed to drive CMOS logic to normal 30% to 70% levels, and incorporates an internal pullup device that remains connected even in the input mode. Because of this, the A side requires more drive current in the input mode than Port B. In contrast, the B side uses a normal three-state NMOS buffer which cannot pullup to CMOS levels without external resistors. The B side can drive extra loads such as Darlingtons without problem. When the PIA comes out of reset, the A port represents inputs with pullup resistors, whereas the B side (input mode also) will float high or low, depending upon the load connected to it.

Notice the differences between a Port A and Port B read operation when in the output mode. When reading Port A, the actual pin is read, whereas the B side read comes from an output latch, ahead of the actual pin.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1, and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on contrtol lines CA1, CA2, CB1, or CB2. The format of the control words is shown in Figure 18.

DATA DIRECTION ACCESS CONTROL BIT (CRA-2 and CRB-2)

Bit 2, in each Control Register (CRA and CRB), determines selection of either a Peripheral Output Register of the corresponding Data Direction E Register when the proper register select signals are applied to RS0 and RS1. A "1" in bit 2 allows access of the Peripheral Interface Register, while a "0" causes the Data Direction Register to be addressed.

Interrupt Flags (CRA-6, CRA-7, CRB-6 and CRB-7) — The four interrupt flag bits are set by active transitions of signals on the four interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) — Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different loading characteristics.

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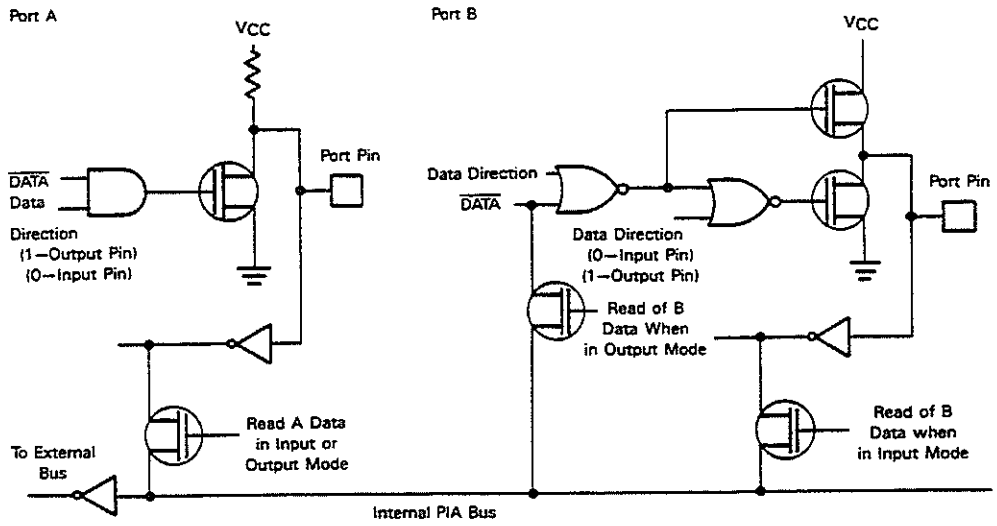
Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) — The two lowest-order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1.

FIGURE 17 — PORT A AND PORT B EQUIVALENT CIRCUITS



ORDERING INFORMATION

MC68A21CP

Motorola Integrated Circuit
M6800 Family
Blanks = 1.0 MHz
A = 1.5 MHz
B = 2.0 MHz
Device Designation
In M6800 Family
Temperature Range
Blank = 0° — +70°C
C = −40° — +85°C
Package
P = Plastic
S = Cerdip
L = Ceramic

BETTER PROGRAM

Better program processing is available on all types listed. Add suffix letters to part number.

Level 1 add "S" Level 2 add "D" Level 3 add "DS"

Level 1 "S" = 10 Temp Cycles — (−25 to 150°C); Hi Temp testing at T_A max.
Level 2 "D" = 168 Hour Burn-in at 125°C
Level 3 "DS" = Combination of Level 1 and 2.

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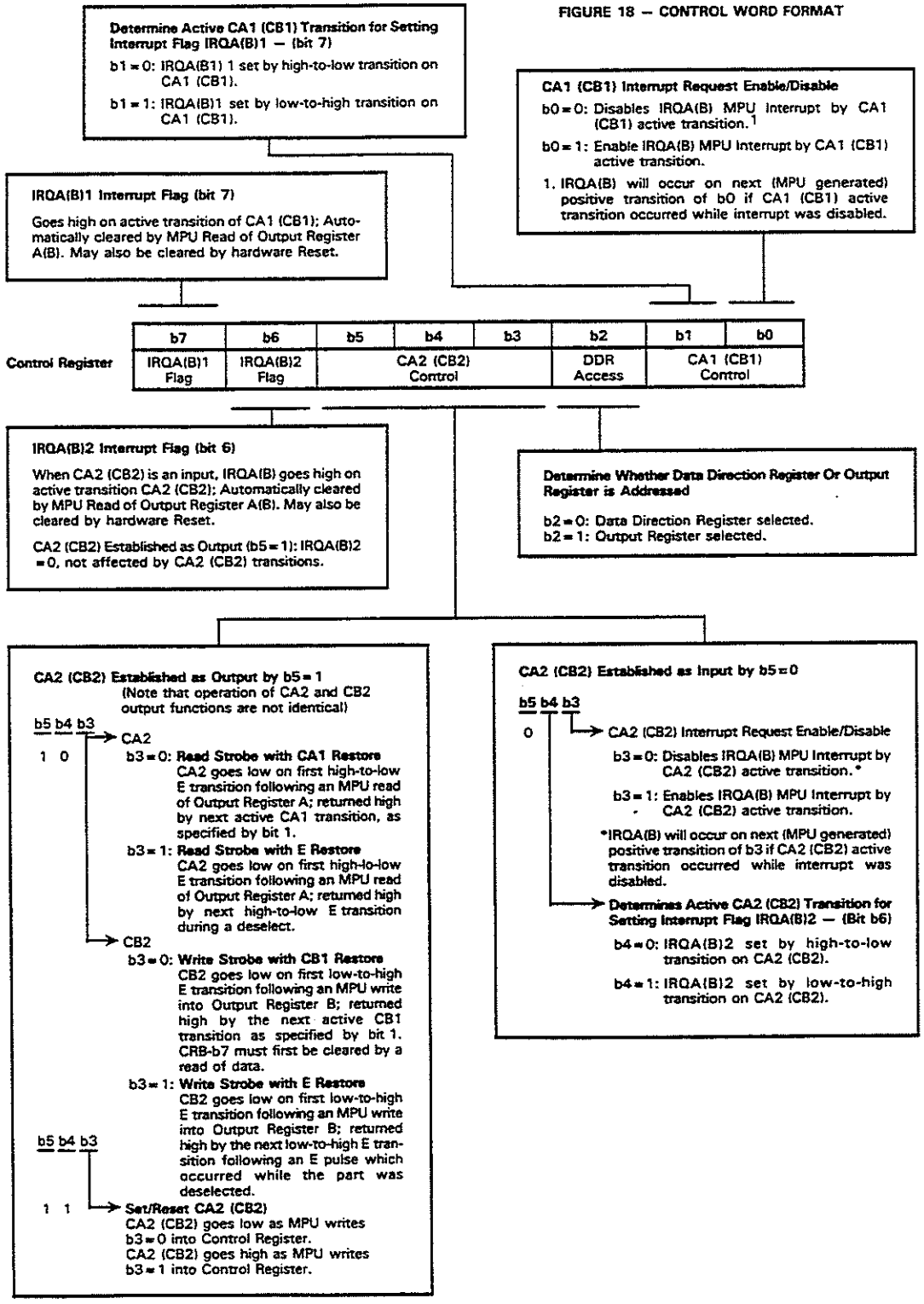
FIGURE 18 — CONTROL WORD FORMAT



Z8470 Z80® DART Dual Asynchronous Receiver/Transmitter

Zilog

Product Specification

April 1985

FEATURES

- Two independent full-duplex channels with separate modem controls. Modem status can be monitored.
- In x1 clock mode, data rates are 0 to 500K bits/second with a 2.5 MHz clock, or 0 to 800K bits/second with a 4.0 MHz clock.
- Receiver data registers are quadruply buffered; the transmitter is doubly buffered.
- Programmable options include 1, 1½, or 2 stop bits; even, odd, or no parity; and x1, x16, x32, and x64 clock modes.
- Break generation and detection as well as parity-, overrun-, and framing-error detection are available.
- Interrupt features include a programmable interrupt vector, a "status affects vector" mode for fast interrupt processing, and the standard Z80 peripheral daisy-chain interrupt structure that provides automatic interrupt vectoring with no external logic.
- On-chip logic for ring indication and carrier-detect status.

GENERAL DESCRIPTION

The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multifunction peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems. The Z80 DART is used as a serial-to-parallel, parallel-to-serial converter/controller in asynchronous applications. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general-purpose I/O.

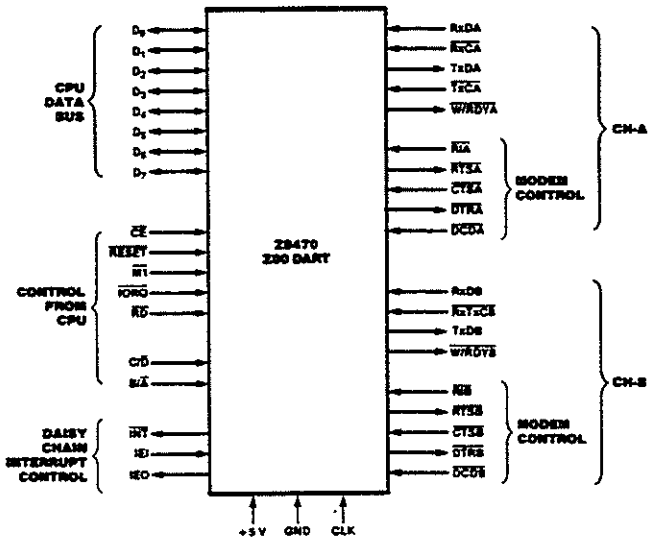


Figure 1. Pin Functions

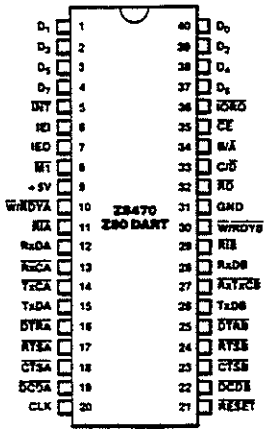


Figure 2. 40-Pin Dual-In-Line Package (DIP), Pin Assignments

Zilog also offers the Z80 SIO, a more versatile device that provides synchronous (Bisync, HDLC, and SDLC) as well as asynchronous operation.

The Z80 DART is fabricated with n-channel silicon-gate depletion-load technology, and is packaged in a 40-pin plastic or ceramic DIP (Figures 1 and 2).

PIN DESCRIPTION

B/$\overline{A}$. *Channel A or B Select* (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the Z80 DART.

C/$\overline{D}$. *Control or Data Select* (input, High selects Control). This input specifies the type of information (control or data) transferred on the data bus between the CPU and the Z80 DART.

$\overline{CE}$. *Chip Enable* (input, active Low). A Low at this input enables the Z80 DART to accept command or data input from the CPU during a write cycle, or to transmit data to the CPU during a read cycle.

CLK. *System Clock* (input). The Z80 DART uses the standard Z80 single-phase system clock to synchronize internal signals.

$\overline{CTSA}$, $\overline{CTSB}$. *Clear To Send* (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals.

D_0-D_7. *System Data Bus* (bidirectional, 3-state). This bus transfers data and commands between the CPU and the Z80 DART.

$\overline{DCDA}$, $\overline{DCDB}$. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if the Z80 DART is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered.

$\overline{DTRA}$, $\overline{DTRB}$. *Data Terminal Ready* (outputs, active Low). These outputs follow the state programmed into the DTR bit. They can also be programmed as general-purpose outputs.

IEI. *Interrupt Enable In* (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this Z80 DART. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. *Interrupt Request* (output, open drain, active Low). When the Z80 DART is requesting an interrupt, it pulls $\overline{INT}$ Low.

$\overline{M1}$. *Machine Cycle One* (input from Z80 CPU, active Low). When $\overline{M1}$ and $\overline{RD}$ are both active, the Z80 CPU is fetching an instruction from memory; when $\overline{M1}$ is active while $\overline{IORQ}$ is active, the Z80 DART accepts $\overline{M1}$ and $\overline{IORQ}$ as an interrupt acknowledge if the Z80 DART is the highest priority device that has interrupted the Z80 CPU.

$\overline{IORQ}$. *Input/Output Request* (input from CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$, and $\overline{RD}$ to transfer commands and data between the CPU and the Z80 DART. When $\overline{CE}$, $\overline{RD}$, and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active, but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$.

$\overline{RxCA}$, $\overline{RxCB}$. *Receiver Clocks* (inputs). Receive data is sampled on the rising edge of RxC. The Receive Clocks may be 1, 16, 32, or 64 times the data rate.

$\overline{RD}$. *Read Cycle Status* (input from CPU, active Low). If $\overline{RD}$ is active, a memory or I/O read operation is in progress.

RxDA, RxDB. *Receive Data* (inputs, active High).

$\overline{RESET}$. *Reset* (input, active Low). Disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High, and disables all interrupts.

$\overline{RIA}$, $\overline{RIB}$. *Ring Indicator* (inputs, active Low). These inputs are similar to CTS and DCD. The Z80 DART detects both logic level transitions and interrupts the CPU. When not used in switched-line applications, these inputs can be used as general-purpose inputs.

$\overline{RTSA}$, $\overline{RTSB}$. *Request to Send* (outputs, active Low). When the RTS bit is set, the RTS output goes Low. When the $\overline{RTS}$ bit is reset, the output goes High after the transmitter empties.

$\overline{TxCA}$, $\overline{TxCB}$. *Transmitter Clocks* (inputs). TxD changes on the falling edge of $\overline{TxC}$. The Transmitter Clocks may be 1, 16, 32, or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered. Both the Receiver and Transmitter Clocks may be driven by the Z80 CTC Counter Time Circuit for programmable baud rate generation.

TxDA, TxDB. *Transmit Data* (outputs, active High).

$\overline{W/RDYA}$, $\overline{W/RDYB}$. *Wait/Ready* (outputs, open drain when programmed for Wait function, driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the Z80 DART data rate. The reset state is open drain.

FUNCTIONAL DESCRIPTION

The functional capabilities of the Z80 DART can be described from two different points of view: as a data communications device, it transmits and receives serial data, and meets the requirements of asynchronous data communications protocols; as a Z80 family peripheral, it interacts with the Z80 CPU and other Z80 peripheral circuits, and shares the data, address, and control buses, as well as being a part of the Z80 interrupt structure. As a peripheral to other microprocessors, the Z80 DART offers valuable features such as nonvectored interrupts, polling, and simple handshake capability.

The first part of the following functional description introduces Z80 DART data communications capabilities; the second part describes the interaction between the CPU and the Z80 DART.

The Z80 DART offers RS-232 serial communications support by providing device signals for external modem control. In addition to dual-channel Request To Send, Clear To Send, and Data Carrier Detect ports, the Z80 DART also features a dual channel Ring Indicator (RIA, RIB) input to facilitate local/remote or station-to-station communication capability. Figure 3 is a block diagram.

Communications Capabilities. The Z80 DART provides two independent full-duplex channels for use as an asynchronous receiver/transmitter. The following is a short description of receiver/transmitter capabilities. For more details, refer to the Asynchronous Mode section of the *Z80 SIO Technical Manual* (03-3033-01).

The Z80 DART offers transmission and reception of five to eight bits per character, plus optional even or odd parity. The transmitter can supply one, one and a half, or two stop bits per character and can provide a break output at any time. The receiver break detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the Receive Data input. If the Low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the character on which they occurred. Vectored interrupts allow fast servicing of interrupting conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit is begun.

The Z80 DART does not require symmetric Transmit and Receive Clock signals, a feature that allows it to be used with a Z80 CTC or any other clock source. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32, or 1/64 of the clock rate supplied to the Receive and Transmit Clock inputs. When using Channel B, the bit rates for transmit and receive operations must be the same because $\overline{RxC}$ and $\overline{TxC}$ are bonded together ($\overline{RxTxCB}$).

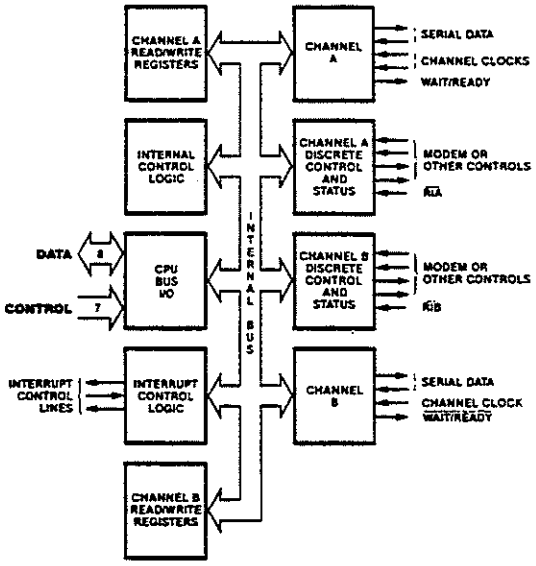


Figure 3. Block Diagram

I/O Interface Capabilities. The Z80 DART offers the choice of Polling, Interrupt (vectored or non-vectored) and Block Transfer modes to transfer data, status, and control information to and from the CPU. The Block Transfer mode can be implemented under CPU or DMA control.

Polling. There are no interrupts in the Polled mode. Status registers RR0 and RR1 are updated at appropriate times for each function being performed. All the interrupt modes of the Z80 DART must be disabled to operate the device in a Polled environment.

While in its Polling sequence, the CPU examines the status contained in RR0 for each channel; the RR0 status bits serve as an acknowledge to the Poll inquiry. The two RR0 status bits D_0 and D_2 indicate that a data transfer is needed. The status also indicates Error or other special status conditions. The Z80 DART Programming section contains more information. The Special Receive Condition status contained in RR1 does not have to be read in a Polling sequence because the status bits in RR1 are accompanied by a Receive Character Available status in RR0.

Interrupts. The Z80 DART offers an elaborate interrupt scheme that provides fast interrupt response in real-time applications. As a member of the Z80 family, the Z80 DART can be daisy-chained along with other Z80 peripherals for peripheral interrupt-priority resolution. In addition, the internal interrupts of the Z80 DART are nested to prioritize the various interrupts generated by Channels A and B. Channel B registers WR2 and RR2 contain the interrupt vector that points to an interrupt service routine in the memory. To eliminate the necessity of writing a status analysis routine, the Z80 DART can modify the interrupt vector in RR2 so it points directly to one of eight interrupt service routines. This is done under program control by setting a program bit (WR1, D_2) in Channel B called "Status

Affects Vector." When this bit is set, the interrupt vector in RR2 is modified according to the assigned priority of the various interrupting conditions.

Transmit interrupts, Receive interrupts, and External/Status interrupts are the main sources of interrupts. Each interrupt source is enabled under program control with Channel A having a higher priority than Channel B, and with Receiver, Transmit, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled, the CPU is interrupted by the transmit buffer becoming empty. (This implies that the transmitter must have had a data character written into it so it can become empty.) When enabled, the receiver can interrupt the CPU in one of three ways:

- Interrupt on the first received character
- Interrupt on all received characters
- Interrupt on a Special receive condition

Interrupt On First Character is typically used with the Block Transfer mode. Interrupt On All Received Characters can optionally modify the interrupt vector in the event of a parity error. The Special Receive Condition interrupt can occur on a character basis. The Special Receive Condition can cause an interrupt can occur on a character basis. The Special Receive condition can cause an interrupt only if the Interrupt On First Received Character or Interrupt On All Received Characters mode is selected. In Interrupt On First Receive Character, an interrupt can occur from Special Receive conditions (except Parity Error) after the first Received character interrupt (example: Receive Overrun interrupt).

The main function of the External/Status interrupt is to monitor the signal transitions of the $\overline{CTS}$, $\overline{DCD}$, and $\overline{RI}$ pins; however, an External/Status interrupt is also caused by the detection of a Break sequence in the data stream. The interrupt caused by the Break sequence has a special feature that allows the Z80 DART to interrupt when the Break sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the Break condition.

CPU/DMA Block Transfer. The Z80 DART provides a Block Transfer mode to accommodate CPU block transfer functions and DMA block transfers (Z80 DMA or other designs). The Block Transfer mode uses the $\overline{W/RDY}$ output in conjunction with the Wait/Ready bits of Write Register 1. The $\overline{W/RDY}$ output can be defined under software control as a Wait line in the CPU Block Transfer mode or as a Ready line in the DMA Block Transfer mode.

To a DMA controller, the Z80 DART Ready output indicates that the Z80 DART is ready to transfer data to or from memory. To the CPU, the Wait output indicates that the Z80 DART is not ready to transfer data, thereby requesting the CPU to extend the I/O cycle.

INTERNAL ARCHITECTURE

The device internal structure includes a Z80 CPU interface, internal control and interrupt logic, and two full-duplex channels. Each channel contains read and write registers, and discrete control and status logic that provides the interface to modems or other external devices.

The read and write register group includes five 8-bit control registers and two status registers. The interrupt vector is written into an additional 8-bit register (Write Register 2) in Channel B, that may be read through Read Register 2 in Channel B. The registers for both channels are designated as follows:

WR0-WR5 Write Registers 0 through 5
RR0-RR2 Read Registers 0 through 2

The bit assignment and functional grouping of each register is configured to simplify and organize the programming process.

The logic for both channels provides formats, bit synchronization, and validation for data transferred to and from the channel interface. The modem control inputs Clear to Send ($\overline{CTS}$), Data Carrier Detect ($\overline{DCD}$), and Ring Indicator ($\overline{RI}$) are monitored by the control logic under program control. All the modem control signals are general purpose in nature and can be used for functions other than modem control.

For automatic interrupt vectoring, the interrupt control logic determines which channel and which device within the channel has the highest priority. Priority is fixed with Channel A assigned a higher priority than Channel B; Receive, Transmit, and External/Status interrupts are prioritized in that order within each channel.

Data Path. The transmit and receive data path illustrated for Channel A in Figure 4 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service a Receive Character Available interrupt in a high-speed data transfer.

The transmitter has an 8-bit transmit data register that is loaded from the internal data bus, and a 9-bit transmit shift register that is loaded from the transmit data register.

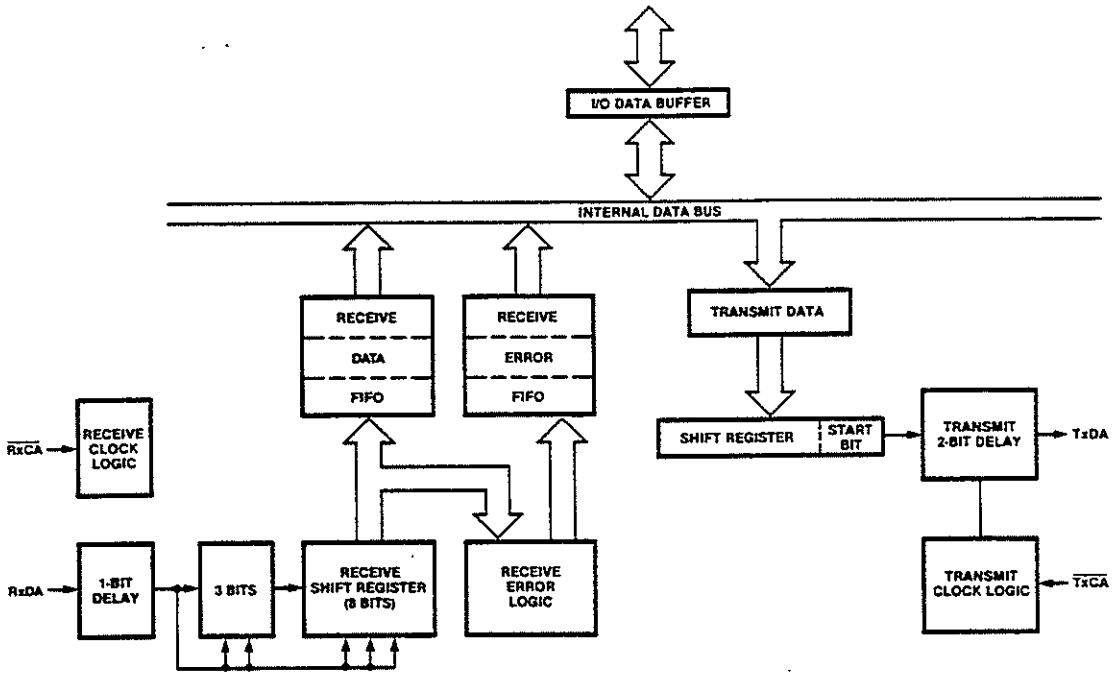


Figure 4. Data Path

READ, WRITE AND INTERRUPT TIMING

Read Cycle. The timing signals generated by a Z80 CPU input instruction to read a Data or Status byte from the Z80 DART are illustrated in Figure 5.

Write Cycle. Figure 6 illustrates the timing and data signals generated by a Z80 CPU output instruction to write a Data or Control byte into the Z80 DART.

Interrupt Acknowledge Cycle. (Figure 7) After receiving an Interrupt Request signal ($\overline{INT}$ pulled Low), the Z80 CPU sends an Interrupt Acknowledge signal ($\overline{M1}$ and $\overline{IORQ}$ both Low). The daisy-chained interrupt circuits determine the highest priority interrupt requestor. The IEI of the highest priority peripheral is terminated High. For any peripheral that has no interrupt pending or under service, IEO = IEI. Any peripheral that does have an interrupt pending or under service forces its IEO Low.

To insure stable conditions in the daisy chain, all interrupt status signals are prevented from changing while $\overline{M1}$ is Low. When $\overline{IORQ}$ is Low, the highest priority interrupt requestor (the one with IEI High) places its interrupt vector on the data bus and sets its internal interrupt-under-service latch.

Refer to the *Technical Manual* (03-3033-01) for additional details on the interrupt daisy chain and interrupt nesting.

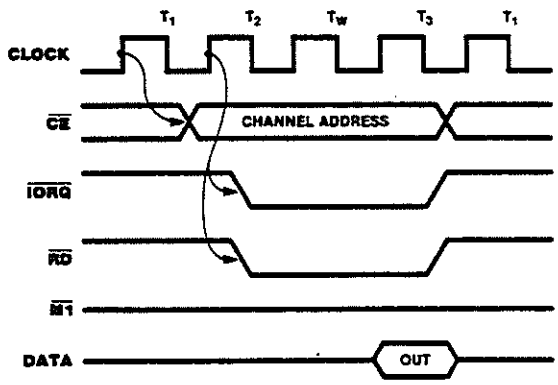


Figure 5. Read Cycle

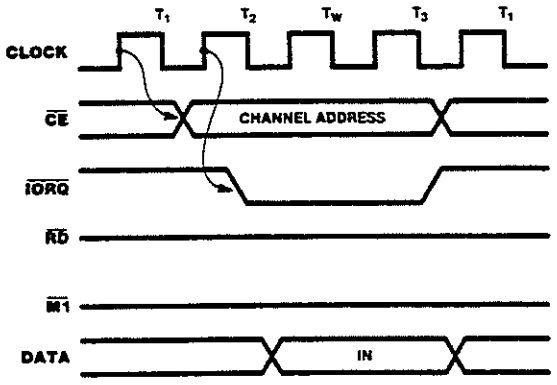


Figure 6. Write Cycle

2044-004, 005, 006

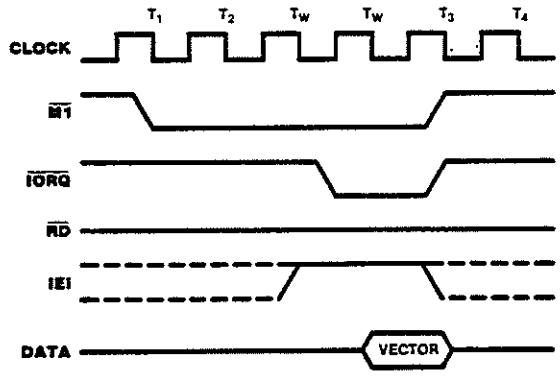


Figure 7. Interrupt Acknowledge Cycle

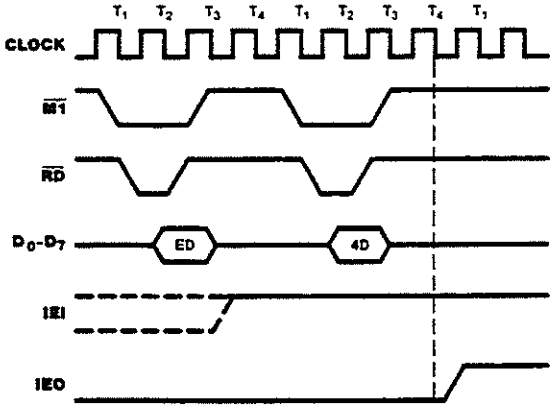


Figure 8. Return from Interrupt Cycle

Return From Interrupt Cycle. (Figure 8) Normally, the Z80 CPU issues an RETI (Return From Interrupt) instruction at the end of an interrupt service routine. RETI is a 2-byte opcode (ED-4D) that resets the interrupt-under-service latch to terminate the interrupt that has just been processed.

When used with other CPUs, the Z80 DART allows the user to return from the interrupt cycle with a special command called "Return From Interrupt" in Write Register 0 of Channel A. This command is interpreted by the Z80 DART in exactly the same way it would interpret an RETI command on the data bus.

Z80 DART PROGRAMMING

To program the Z80 DART, the system program first issues a series of commands that initialize the basic mode and then other commands that qualify conditions within the selected mode. For example, the character length, clock rate, number of stop bits, even or odd parity are first set, then the interrupt mode and, finally, receiver or transmitter enable.

Both channels contain command registers that must be programmed via the system program prior to operation. The Channel Select input (B/$\overline{A}$) and the Control/Data input (C/$\overline{D}$) are the command structure addressing controls, and are normally controlled by the CPU address bus.

Write Registers. The Z80 DART contains six registers (WR0-WR5) in each channel that are programmed separately by the system program to configure the functional personality of the channels (Figure 4). With the exception of WR0, programming the write registers requires two bytes. The first byte contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the Z80 DART.

WR0 is a special case in that all the basic commands (CMD_0-CMD_2) can be accessed with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This means that a register cannot be pointed to in the same operation as a channel reset.

Write Register Functions	
WR0	Register pointers, initialization commands for the various modes
WR1	Transmit/Receive interrupt and data transfer mode definition
WR2	Interrupt vector (Channel B only)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls

Read Registers. The Z80 DART contains three registers (RR0-RR2) that can be read to obtain the status information for each channel (except for RR2, which applies to Channel B only). The status information includes error conditions, interrupt vector, and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing an input instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occurred, all the appropriate error bits can be read from a single register (RR1).

Read Register Functions	
RR0	Transmit/Receive buffer status, interrupt status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only)

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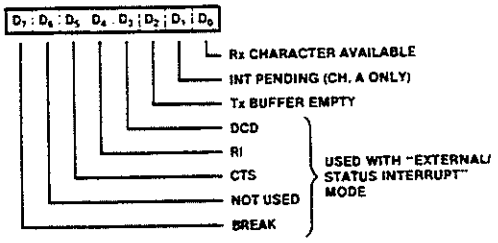
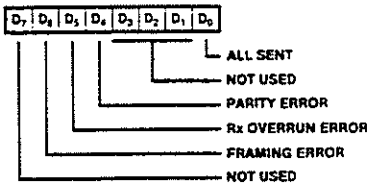
Z80 DART READ AND WRITE REGISTERS

READ REGISTER 0

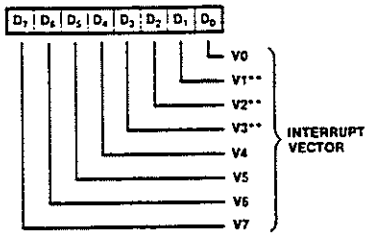


READ REGISTER 1 *



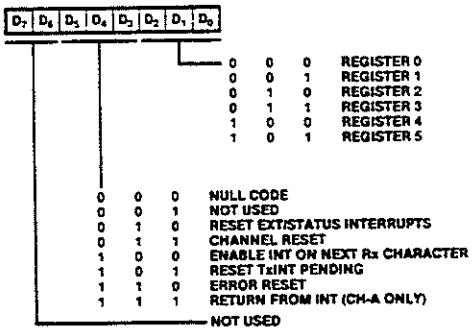
*Used With Special Receive Condition Mode.

READ REGISTER 2

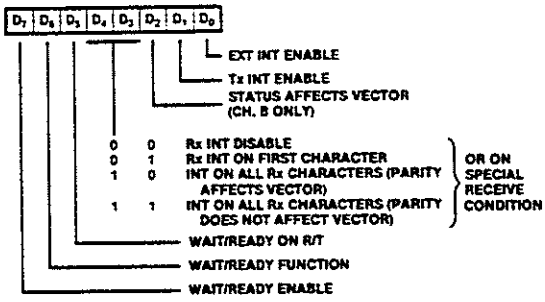


**Variable if "Status Affects Vector" is Programmed.

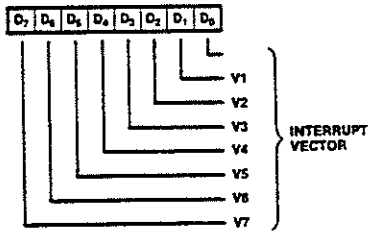
WRITE REGISTER 0



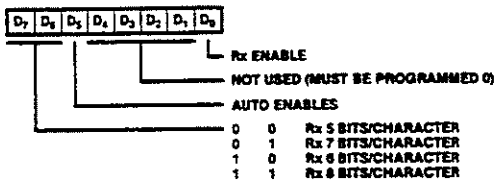
WRITE REGISTER 1



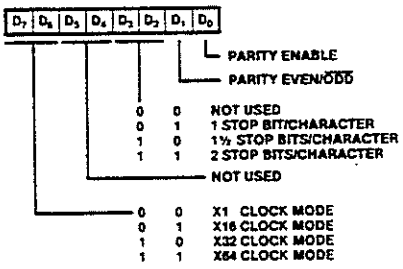
WRITE REGISTER 2 (Channel B only)



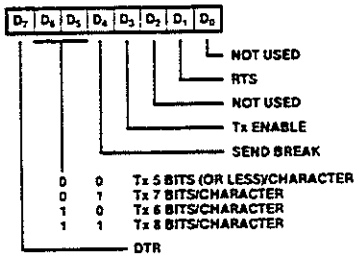
WRITE REGISTER 3



WRITE REGISTER 4



WRITE REGISTER 5



ABSOLUTE MAXIMUM RATINGS

Voltages on all pins with respect to GND ..... −0.3V to +7V
Operating Ambient Temperature ..... See Ordering Information
Storage Temperature ..... −65°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

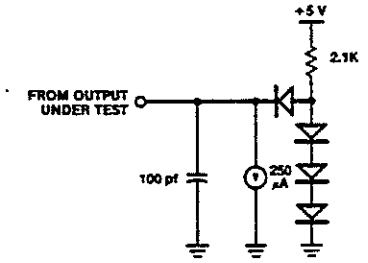
STANDARD TEST CONDITIONS

The DC characteristics and capacitance sections listed below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:

- S = 0°C to +70°C, $+4.75V \leq V_{CC} \leq +5.25V$
- E = −40°C to +85°C, $+4.75V \leq V_{CC} \leq +5.25V$
- M = −55°C to +125°C, $+4.5V \leq V_{CC} \leq +5.5V$

The Ordering Information section lists package temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.



DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	−0.3	+0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−0.6	+5.5	V	
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.0	+5.5	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	+2.4		V	I_{OH} = −250 µA
I_L	Input/3-State Output Leakage Current	−10	+10	µA	$0.4 < V_{IN} < 2.4V$
$I_{L(RI)}$	RI Pin Leakage Current	−40	+10	µA	$0.4 < V_{IN} < 2.4V$
I_{CC}	Power Supply Current		100	mA	

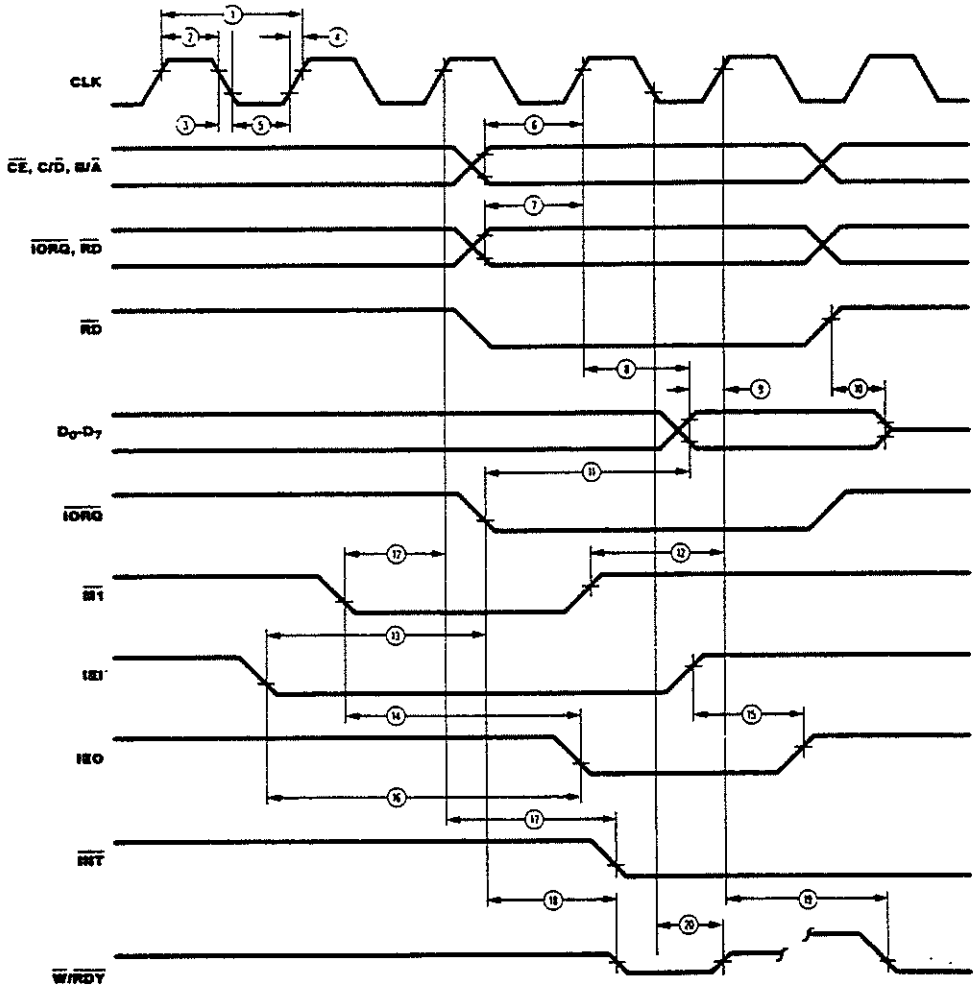
T_A = 0°C to 70°C, V_{CC} = +5V, ±5%.

CAPACITANCE

Symbol	Parameter	Min	Max	Unit
C	Clock Capacitance		40	pf
C_{IN}	Input Capacitance		5	pf
C_{OUT}	Output Capacitance		15	pf

Over specified temperature range; f = 1 MHz.
Unmeasured pins returned to ground.

AC CHARACTERISTICS TIMING

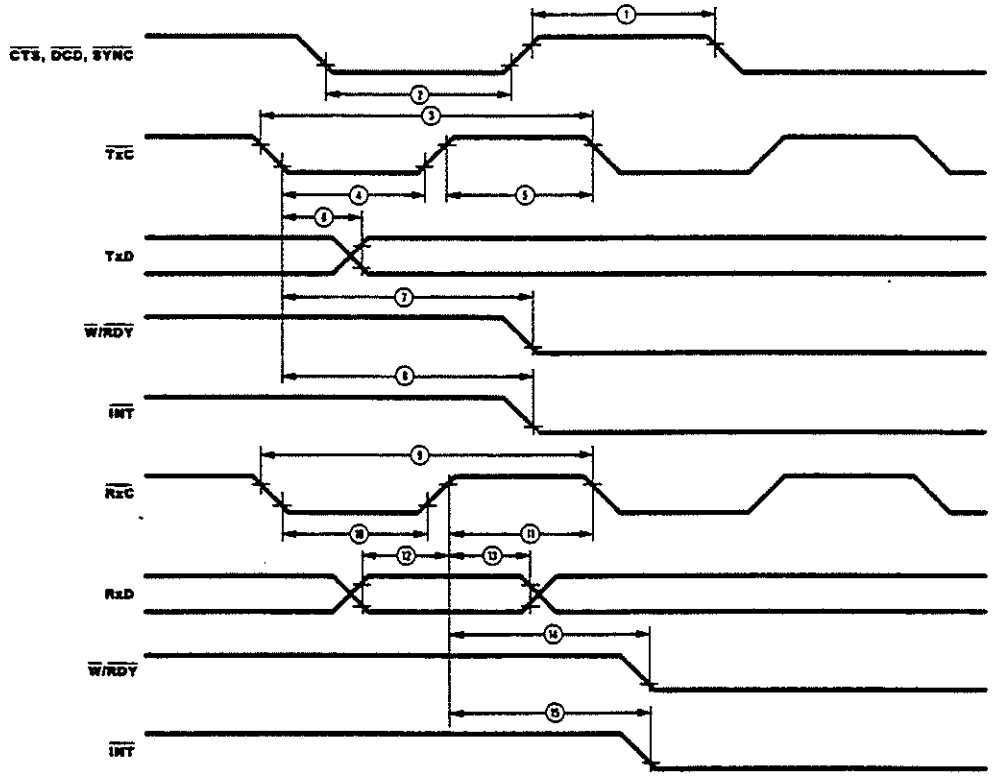


AC CHARACTERISTICS

Number	Symbol	Parameter	Z80 DART Min	Z80 DART Max	Z80A DART Min	Z80A DART Max	Z80B DART* Min	Z80B DART* Max
1	TcC	Clock Cycle Time	400	4000	250	4000	165	4000
2	TwCh	Clock Width (High)	170	2000	105	2000	70	2000
3	TfC	Clock Fall Time		30		30		15
4	TrC	Clock Rise Time		30		30		15
5	TwCl	Clock Width (Low)	170	2000	105	2000	70	2000
6	TsAD(C)	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to Clock ↑ Setup Time	160		145		60	
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup Time	240		115		60	
8	TdC(DO)	Clock ↑ to Data Out Delay		240		220		150
9	TsDI(C)	Data In to Clock ↑ Setup (Write or M1 Cycle)	50		50		30	
10	TdRD(DOz)	$\overline{RD}$ ↑ to Data Out Float Delay		230		110		90
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay (INTACK Cycle)		340		160		100
12	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	210		90		75	
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time (INTACK Cycle)	200		140		120	
14	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (interrupt before M1)		300		190		160
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		150		100		70
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		150		100		70
17	TdC(INT)	Clock ↑ to INT ↓ Delay		200		200		150
18	TdIO(W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Wait Mode)		300		210		175
19	TdC(W/RR)	Clock ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)		120		120		100
20	TdC(W/RWz)	Clock ↓ to $\overline{W/RDY}$ Float Delay (Wait Mode)		150		130		110

*Units in nanoseconds (ns).

AC CHARACTERISTICS (Continued)



Number	Symbol	Parameter	Z80 DART Min	Z80 DART Max	Z80A DART Min	Z80A DART Max	Z80B DART Min	Z80B DART Max	Notes*
1	TwPh	Pulse Width (High)	200		200		200		2
2	TwPl	Pulse Width (Low)	200		200		200		2
3	TcTxC	$\overline{TxC}$ Cycle Time	400	∞	400	∞	330	∞	2
4	TwTxCl	$\overline{TxC}$ Width (Low)	180	∞	180	∞	100	∞	2
5	TwTxCh	$\overline{TxC}$ Width (High)	180	∞	180	∞	100	∞	2
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay		400		300		220	2
7	TdTxC(W/RRf)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	5	9	5	9	5	9	1
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	5	9	1
9	TcRxC	$\overline{RxC}$ Cycle Time	400	∞	400	∞	330	∞	2
10	TwRxCl	$\overline{RxC}$ Width (Low)	180	∞	180	∞	100	∞	2
11	TwRxCh	$\overline{RxC}$ Width (High)	180	∞	180	∞	100	∞	2
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (x1 Mode)	0		0		0		2
13	ThRxD(RxC)	RxD Hold Time (x1 Mode)	140		140		100		2
14	TdRxC(W/RRf)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10	13	10	13	10	13	1
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10	13	10	13	10	13	1

* In all modes, the System Clock rate must be at least five times the maximum data rate. $\overline{RESET}$ must be active a minimum of one complete clock cycle.
1. Units equal to System Clock Periods.
2. Units in nanoseconds (ns).

ORDERING INFORMATION

Z80 DART, 2.5 MHz
40-pin DIP
Z8470 PS
Z8470 CS
Z8470 PE
Z8470 CE

Z80A DART, 4.0 MHz
40-pin DIP
Z8470A PS
Z8470A CS
Z8470A PE
Z8470A CE

Z80B DART, 6.0 MHz
40-pin DIP
Z8470B PS
Z8470B CS

Codes

First letter is for package; second letter is for temperature.

C = Ceramic DIP
P = Plastic DIP
L = Ceramic LCC
V = Plastic PCC

R = Protopack
T = Low Profile Protopack
DIP = Dual-In-Line Package
LCC = Leadless Chip Carrier
PCC = Plastic Chip Carrier (Leaded)

TEMPERATURE
S = 0°C to +70°C
E = −40°C to +85°C
M* = −55°C to +125°C

FLOW
B = 883 Class B

Example: PS is a plastic DIP, 0°C to +70°C.

†Available soon.
*For Military Orders, contact your local Zilog Sales Office for Military Electrical Specifications.

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