



# MP7682/XRD7682

CMOS  
6-Bit High Speed  
Analog-to-Digital Converter

January 1996-2

## FEATURES

- Sampling Rates from 0.001 to 15 MHz (MSPS)
- Interface to any Input Range between GND and  $V_{DD}$
- Pipeline Mode
- Monotonic; No Missing Codes
- Single Power Supply (4 to 6 volt)
- Low Power CMOS (135 mW typ.)
- ESD Protection: 4000 Volts Minimum
- Latch-Up Free

## BENEFITS

- Highest Conversion Speed at Low Power
- Most Flexible Input Range of any A/D Available
- No Sample/Hold Needed
- Easy Ping-Ponging for 30 MSPS System

## GENERAL DESCRIPTION

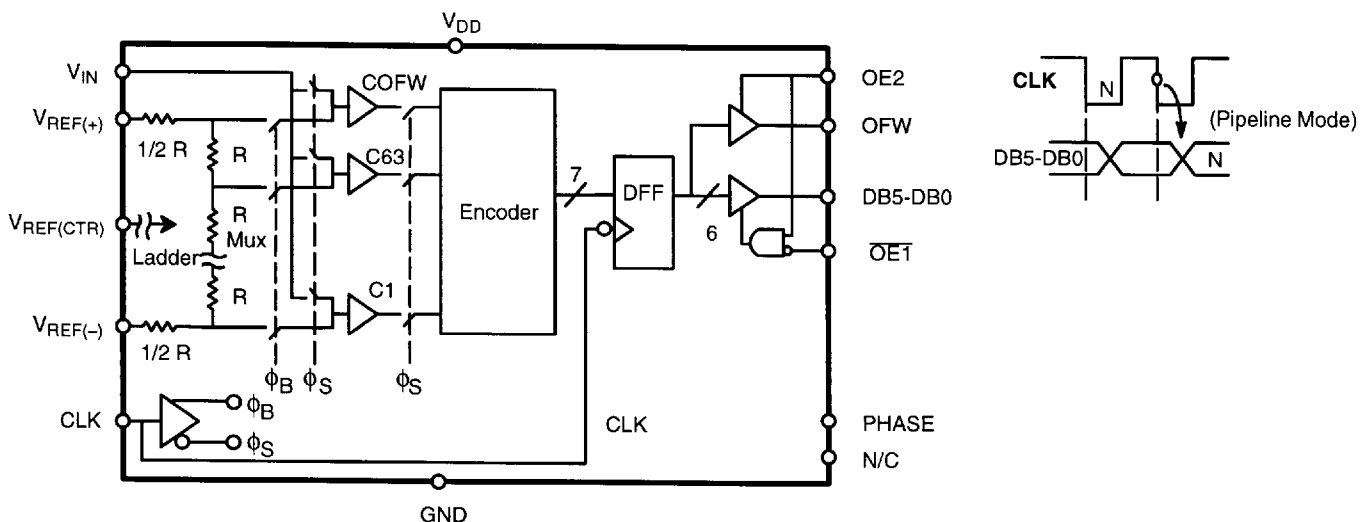
The MP7682/XRD7682 is a 6-bit monolithic CMOS single step high speed Analog-to-Digital Converter designed for precision 6-bit applications in video, scanning and data acquisition requiring conversion rates to 15 MHz. Differential Linearity error is less than 1/2 LSB at 10 MHz, and power consumption is 135 mW typical.

Another feature of MP7682/XRD7682 is its unique input architecture which eliminates the need for an input track and

hold and allows full scale input ranges from about 1 to 5 volts peak-to-peak, referred to ground or offset. The user simply sets  $V_{REF(-)}$  and  $V_{REF(+)}$  to encompass the desired input range.

MP7682/XRD7682 includes 64 auto-balanced clocked comparators, an encoder, 3-state output buffers, a reference resistor ladder, and associated timing circuitry. An overflow bit (or flag) has been provided to make it possible to achieve 7-bit resolution by connecting two devices in parallel. In normal operation, this flag has no effect on the data bits.

## SIMPLIFIED BLOCK AND TIMING DIAGRAM



Rev. 3.00

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EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ♦ (510) 668-7000 ♦ (510) 668-7010

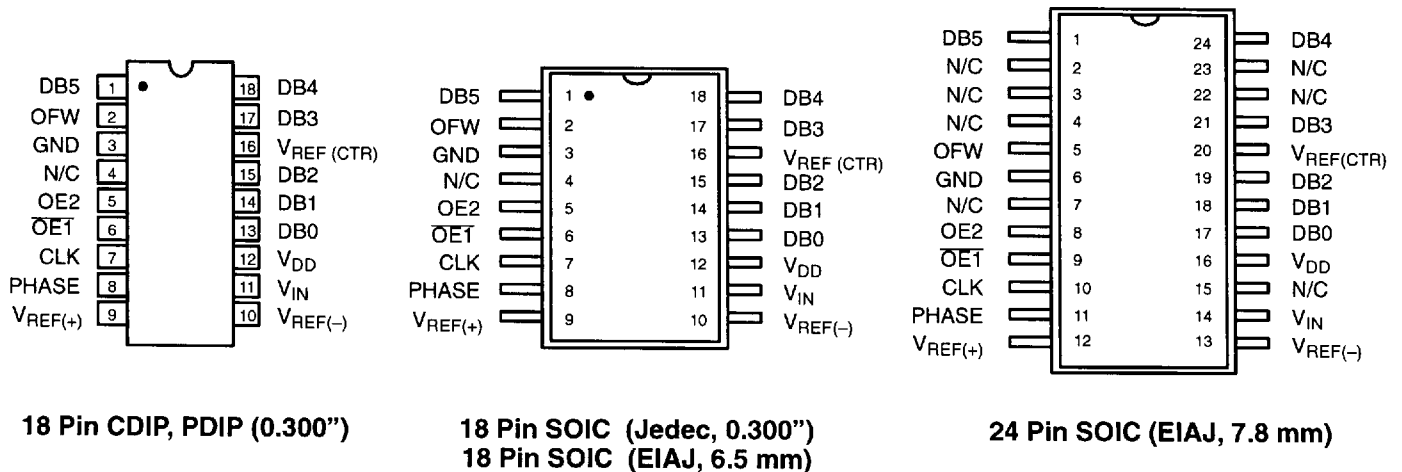


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## ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
Plastic Dip	-40 to +85°C	MP7682JN	±2	2
Plastic Dip	-40 to +85°C	MP7682KN	±1	1
SOIC (Jedec)	-40 to +85°C	MP7682JS	±2	2
SOIC (Jedec)	-40 to +85°C	MP7682KS	±1	1
SOIC (18 Lead EIAJ)	-40 to +85°C	XRD7682AIK18-J	±2	2
SOIC (24 Lead EIAJ)	-40 to +85°C	XRD7682AIK24-J	±2	2
Ceramic Dip	-55 to +125°C	MP7682SD	±2	2

## PIN CONFIGURATIONS



## PIN OUT DEFINITIONS

18 PIN PKG.	24 PIN PKG.	NAME	DESCRIPTION
1	1	DB5	Data Output Bit 5 (MSB)
2	5	OFW	Digital Output Overflow
3	6	GND	Ground
4	2, 3, 4, 7, 15, 22, 23	N/C	N/C
5	8	OE2	Output Enable Control
6	9	OE1	Output Enable Control
7	10	CLK	Clock Input
8	11	PHASE	Sampling Clock Phase Control
9	12	V <sub>REF</sub> (+)	Positive Reference Voltage Pin

18 PIN PKG.	24 PIN PKG.	NAME	DESCRIPTION
10	13	V <sub>REF</sub> (-)	Negative Reference Voltage Pin
11	14	V <sub>IN</sub>	Analog Input
12	16	V <sub>DD</sub>	Power Supply
13	17	DB0	Data Output Bit 0 (LSB)
14	18	DB1	Data Output Bit 1
15	19	DB2	Data Output Bit 2
16	20	V <sub>REF</sub> (CTR)	R Ladder Mid Point
17	21	DB3	Data Output Bit 3
18	24	DB4	Data Output Bit 4

## ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified:  $V_{DD} = 5\text{ V}$ ,  $F_S = 15\text{ MHz}$  (Duty Cycle: 1/3 Sample, 2/3 Balance),  
 $V_{REF(+)} = 4.6$ ,  $V_{REF(-)} = \text{GND}$ ,  $T_A = 25^\circ\text{C}$

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments	
		Min	Typ	Max	Min	Max			
<b>KEY FEATURES</b>									
Resolution		6			6		Bits	For specified accuracy	
Sampling Rate	$F_S$	0.001		15	0.001	15	MHz		
<b>ACCURACY (J, S Grades)<sup>1</sup></b>									
Differential Non-Linearity	DNL			$\pm 1$		$\pm 2$	LSB	Best Fit Line (Max INL – Min INL) / 2	
Integral Non-Linearity (Relative Accuracy)	INL			1		2	LSB		
Zero Scale Error	EZS			$\pm 2$			LSB		
Full Scale Error	EFS			$\pm 2$			LSB		
<b>ACCURACY (K, T Grades)<sup>1</sup></b>									
Differential Non-Linearity	DNL			$\pm 1/2$		$\pm 1$	LSB	Best Fit Line	
Integral Non-Linearity	INL			3/4		1	LSB		
Zero Scale Error	EZS			$\pm 2$			LSB		
Full Scale Error	EFS			$\pm 2$			LSB		
<b>REFERENCE VOLTAGES</b>									
Positive Ref. Voltage	$V_{REF(+)}$			$V_{DD}$		$V_{DD}$	V		
Negative Ref. Voltage	$V_{REF(-)}$	GND			GND		V		
Differential Ref. Voltage <sup>3</sup>	$V_{REF}$	1.0		$V_{DD}-\text{GND}$	1.0	$V_{DD}-\text{GND}$	V		
Ladder Resistance	$R_L$	175	230	270	160	300	$\Omega$		
Ladder Temp. Coefficient <sup>2</sup>	$R_{TCO}$					3000	ppm/°C		
<b>ANALOG INPUT<sup>2</sup></b>									
Input Voltage Range	$V_{IN}$	$V_{REF(-)}$		$V_{REF(+)}$	$V_{REF(-)}$	$V_{REF(+)}$	V p-p	See Figure 5.	
Input Capacitance <sup>5</sup>	$C_{IN}$		20				pF		
Aperture Delay	$t_{AP}$		15				ns		
Aperture Uncertainty (Jitter)	$t_{AJ}$		50				ps		
Clock Kickback Pulse			10				pAs		
<b>DIGITAL INPUTS</b>									
Logical "1" Voltage	$V_{IH}$	2			2		V	$V_{IN}=\text{GND to } V_{DD}$	
Logical "0" Voltage	$V_{IL}$			0.8		0.8	V		
Leakage Currents <sup>6</sup>	$I_{IN}$								
CLK		-1		1	-1	1	$\mu\text{A}$		
OE2		-20		1	-20	1	$\mu\text{A}$		
Phase		-20		1	-20	1	$\mu\text{A}$		
$\overline{\text{OE1}}$		-1		20	-1	20	$\mu\text{A}$		
Input Capacitance <sup>2</sup>	$C_{IND}$		5				pF		
Clock Timing (See Figure 1.)									
Clock Period	$t_S$	50			66		ns		
Rise & Fall Time	$t_R, t_F$			5		5			
"High" Time (Auto-Balance)	$t_H$	25			33		ns		
"Low" Time (Sampling)	$t_L$	25	500,000		33	500,000	ns		

## ELECTRICAL CHARACTERISTICS TABLE CONT'D

Parameter	Symbol	25°C			Tmin to Tmax		Units	Test Conditions/Comments
		Min	Typ	Max	Min	Max		
<b>DIGITAL OUTPUTS</b>								
Logical "1" Voltage	$V_{OH}$	$V_{DD}-0.5$			$V_{DD}-0.5$		V	$I_{LOAD} = 4 \text{ mA}$ $I_{LOAD} = 2.0 \text{ mA}$ $V_{OUT} = \text{GND to } V_{DD}$
Logical "0" Voltage	$V_{OL}$			0.4		0.4	V	
3-state Leakage	$I_{OZ}$	-10		10	-15	15	$\mu\text{A}$	
Data Enable Delay	$t_{DEN}$		18	22		25	ns	
Data 3-state Delay	$t_{DHZ}$		18	22		25	ns	
Pipeline Mode (See Figure 6.) Data Hold Time <sup>2</sup>	$t_{HLD}$	15	22		15		ns	
Data Valid Delay <sup>2</sup>	$t_{DL}$		30	40		40	ns	
<b>POWER SUPPLIES</b>								
Operating Voltage	$V_{DD}$	4		6	4	6	V	
Current	$I_{DD}$		27	35		40	mA	
<b>AC PARAMETERS<sup>2</sup></b>								
Signal Noise Ratio <sup>10</sup>	SNR		36				dB	RMS/RMS Measures $F_{IN} = 5 \text{ MHz}$
Harmonic Distortion								
Second Harmonic	2nd HD		35				-dB	$F_{IN} = 1 \text{ MHz}$
Third Harmonic	3rd HD		35				-dB	$F_{IN} = 5 \text{ MHz}$
Total Harmonic Distortion <sup>12</sup>	THD		29				-dB	$F_{IN} = 5 \text{ MHz}$
Total Dynamic Error <sup>11</sup>	TDE		30				dB	$F_{IN} = 5 \text{ MHz}$
Differential Gain Error	$d_G$		2				%	$F_S = 3 \times \text{NTSC}$
Differential Phase Error	$d_{PH}$		1				Degree	

### NOTES

- 1 Tester measures code transitions by dithering the voltage of the analog input ( $V_{IN}$ ). The difference between the measured and the ideal code width ( $V_{REF}/64$ ) is the DNL error (Figure 3.). The INL error is the maximum distance (in LSBs) from the Best Fit Line to any transition voltage (Figure 4.). Accuracy is a function of the sampling rate ( $F_S$ ).
- 2 Guaranteed. Not tested.
- 3 Specified values guarantee functionality. Refer to other parameters for accuracy.
- 4 Input bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.  
BW calculation:  $BW = V_{OUT} / V_{IN}$   
 $V_{OUT} = V_{REF} * (\text{CODE}_{MAX} - \text{CODE}_{MIN}) / 64$
- 5 See  $V_{IN}$  input equivalent circuit (Figure 5.) for high sampling rates. Switched capacitor analog input requires driver with low output resistance.
- 6 All inputs have diodes to  $V_{DD}$  and GND. Inputs OE2, Phase, Mode have internal pull ups. Input OE1 has internal pull down. Input DC currents will not exceed specified limits for any input voltage between GND and  $V_{DD}$ .
- 7 Internal resistor to  $V_{DD}$  biases unconnected input to active high logical level.
- 8 Internal resistor to GND biases unconnected input to active low logical level.
- 9 Condition to meet aperture delay specifications ( $t_{AP}$ ,  $t_{AJ}$ ). Actual rise/fall time can be less stringent with no loss of accuracy.
- 10 SNR: Ratio of fundamental over noise.
- 11 TDE: Ratio of fundamental over noise + harmonics (2nd to 9th).
- 12 THD: Ratio of harmonics (2nd to 9th) over fundamental.

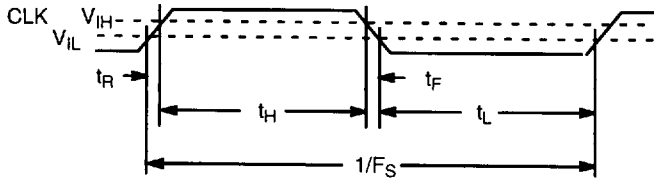
Specifications are subject to change without notice

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25°C unless otherwise noted)<sup>1, 2</sup>**

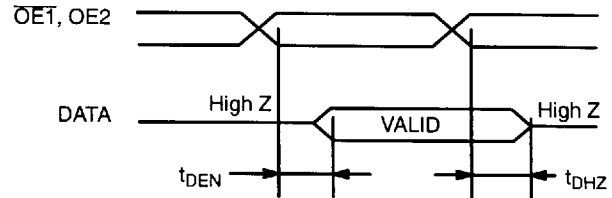
V <sub>DD</sub> to GND .....	+7 V	Storage Temperature .....	-65°C to +150°C
V <sub>REF(+)</sub> & V <sub>REF(-)</sub> .....	GND -0.5 to V <sub>DD</sub> +0.5 V	Lead Temperature (Soldering 10 seconds) ..	+300°C
V <sub>IN</sub> .....	GND -0.5 to V <sub>DD</sub> +0.5 V	Package Power Dissipation Rating to 75°C	
Digital Inputs .....	GND -0.5 to V <sub>DD</sub> +0.5 V	CDIP, PDIP, SOIC .....	850mW
Digital Outputs .....	GND -0.5 to V <sub>DD</sub> +0.5 V	Derates above 75°C .....	11mW/°C

**NOTES:**

- 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- 2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.



**Figure 1. Clock Timing Specification**



**Figure 2. Data Line Enable Delay**

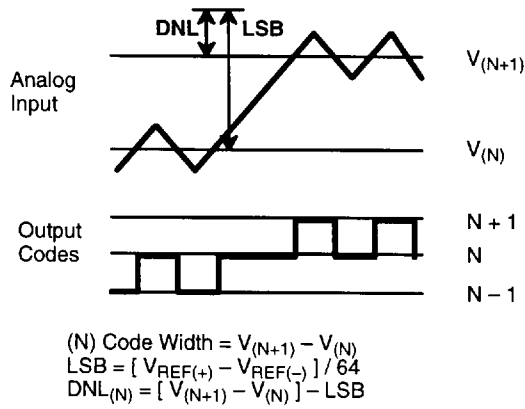


Figure 3. DNL Measurement

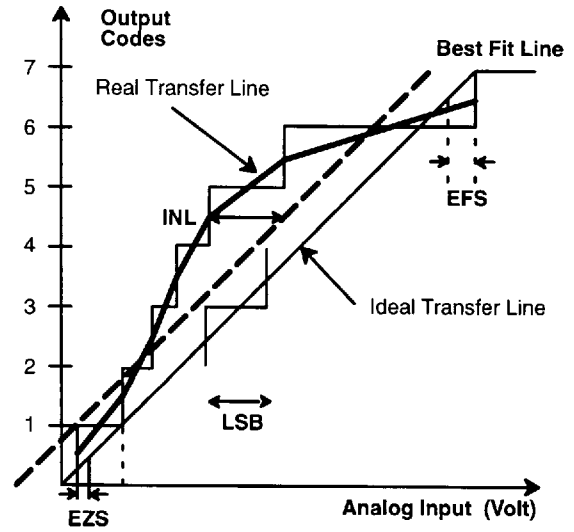


Figure 4. INL Error Calculation

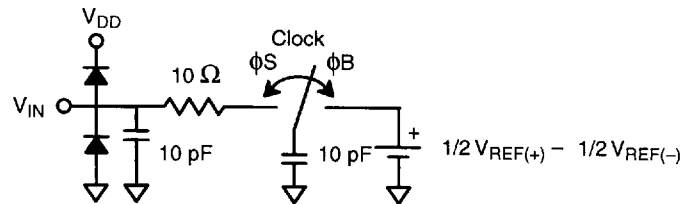
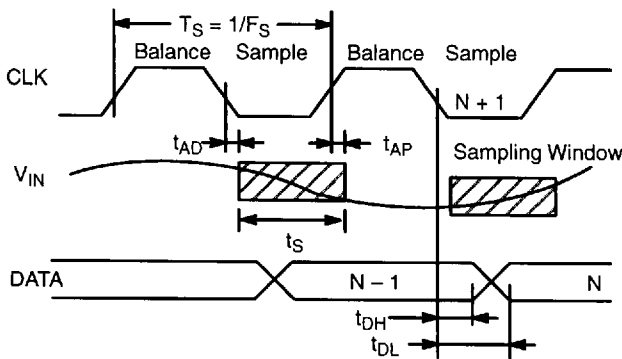


Figure 5. Analog Input Equivalent Circuit

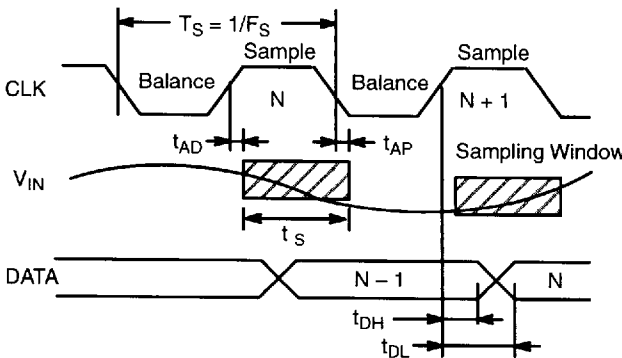
**THEORY OF OPERATION**

**Pipeline Mode**

In this configuration, the MP7682/XRD7682 works in a continuous fashion. Figure 6. shows the timing with the Phase pin high and low. When Phase is low, "sampling" occurs during the low period of the clock, and "balancing" during the high period. When Phase is high, operation is reversed (see Figure 7.), "sampling" occurs during the high period and "balancing" during the low period. The actual time when the internal comparators are connected to  $V_{IN}$  is called the Acquisition Time. This time is equal to the sample phase of the external clock delayed by  $t_{AD}$  and  $t_{AP}$



**Figure 6. Pipeline Mode Timing (Phase = 0)**



**Figure 7. Pipeline Mode Timing (Phase = 1)**

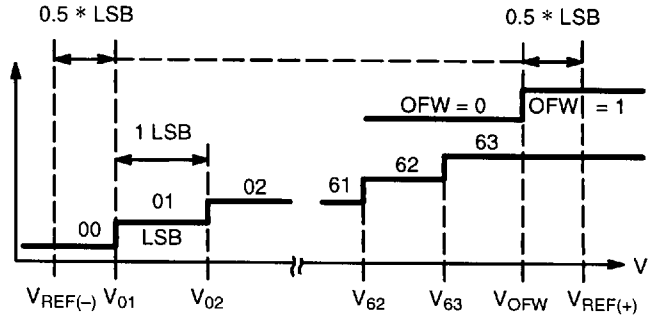
The MP7682/XRD7682 converts analog voltages into 64 digital codes by encoding the outputs of comparators. A comparator is used to generate the overflow bit. The conversion is synchronous with the sample clock. A complete conversion cycle is accomplished in 1.5 cycles. Data is transferred from the comparator latches to the output register each cycle and at the same time the input is sampled.

The clock signal generates the two internal phases,  $\phi_B$  (CLK high = balance) and  $\phi_S$  (CLK low = sample). Phase B connects the comparators to the reference tap points. Phase S connects the comparators to the analog input voltage.

The reference resistance ladder is a series of 65 resistors. The first and the last resistors of the ladder are half the value of the others so that the following relations apply:

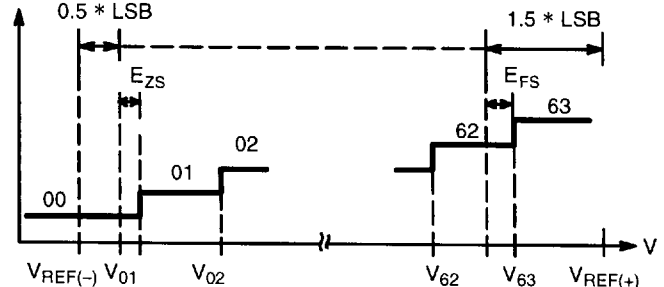
$$R_{REF} = R * 64 \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 64 * LSB$$

**DIGITAL CODES**



**Figure 8. Ideal A/D Transfer Function**

**DIGITAL CODES**



**Figure 9. Real A/D Transfer Curve**

For MP7682/XRD7682 the overflow flag is ideally set at

$$V_{OFW} = V_{REF(+)} - 0.5 * LSB$$

Thus the first and last transition of the data bits take place at

$$V_{IN} = V_{01} = V_{REF(-)} + 0.5 * LSB$$

$$V_{IN} = V_{63} = V_{REF(+)} - 1.5 * LSB$$

$$LSB = (V_{63} - V_{01}) / 62$$

MP7682/XRD7682 also has zero scale and full scale errors which indicate the deviations from the ideal initial and final transitions, thus the various error relationships for Differential Non-Linearity (DNL), Integral Non-Linearity (INL) and the zero and full scale errors (EzS and EFS) can be described as follows:

$$DNL (01) = V_{02} - V_{01} - LSB$$

:::

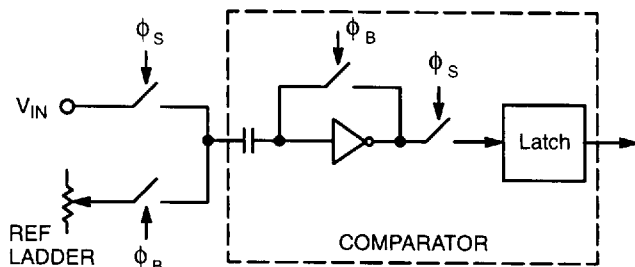
$$DNL (62) = V_{63} - V_{62} - LSB$$

$$E_{FS} \text{ (full scale error)} = V_{63} - [V_{REF(+)} - 1.5 * \text{LSB}]$$

$$E_{ZS} \text{ (zero scale error)} = V_{01} - [V_{REF(-)} + 0.5 * \text{LSB}]$$

$$\text{INL (i)} = \sum \text{DNL (i)}$$

Systems that adjust the  $V_{REF}$  voltages only increase the DNL accuracy at the two extreme points. In the MP7682/XRD7682, such adjustments have little impact at frequencies lower than 15 MHz.



**Figure 10. MP7682/XRD7682 Comparator**

The MP7682/XRD7682 uses the balance phase ( $\phi_B$ ) to charge one plate of the capacitors to the reference ladder tap point and the other to the inverter/comparator trigger point (Figure 10). During the sample phase ( $\phi_S$ ), one plate of the capacitors switches to  $V_{IN}$ . The change in voltage ( $V_{IN} - V_{TAP}$ ) transfers across the capacitor and forces the inverter into one of the two possible logic states. A latch (connected to the comparator during  $\phi_S$ ) restores and propagates the digital level to the decode logic.

The rising edge of the CLK input marks the end of the sampling phase ( $\phi_S$ ). Internal delay of the clock circuitry will delay the actual instant when  $\phi_S$  disconnects the latch from the comparator. This delay is called aperture delay ( $t_{AP}$ ).

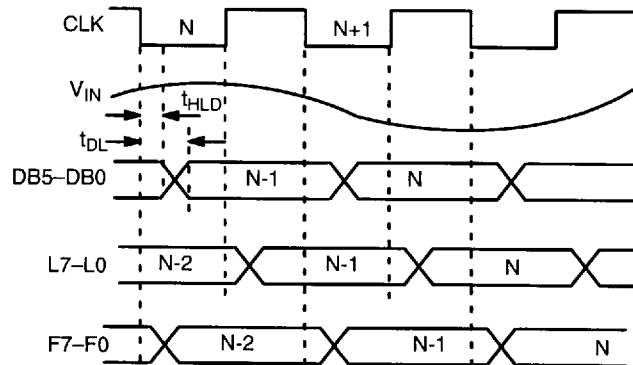
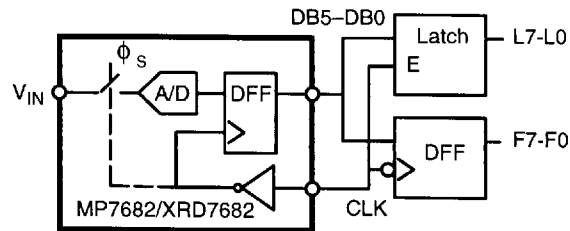
The aperture delay is not constant but changes from one cycle to the next. Internal thermal noise and slow input clock edges are major contributors to this variation. The aperture jitter ( $t_{AJ}$ ) is the variation of the aperture delay distribution.

This uncertainty shows as digital code errors if the input slew rate multiplied by  $t_{AJ}$  is of the same order of magnitude as the LSB. That is, if  $(dv/dt) * t_{AJ} \approx V_{REF}/64$ , an internal 1 LSB of error results.

The logic encodes the 64 bits into a binary code and latches the data in a D-type flip-flop for output. The inputs  $\overline{OE1}$  and  $OE2$  control the output buffers in an asynchronous mode.

$\overline{OE1}$	$OE2$	OFW	DB5 - DB0
X	0	High Z	High Z
1	1	Valid	High Z
0	1	Valid	Valid

**Table 1. Output Enable Logic**



**Figure 11. MP7682/XRD7682 Functional Equivalent Circuit and Interface Timing (Pipeline Mode)**

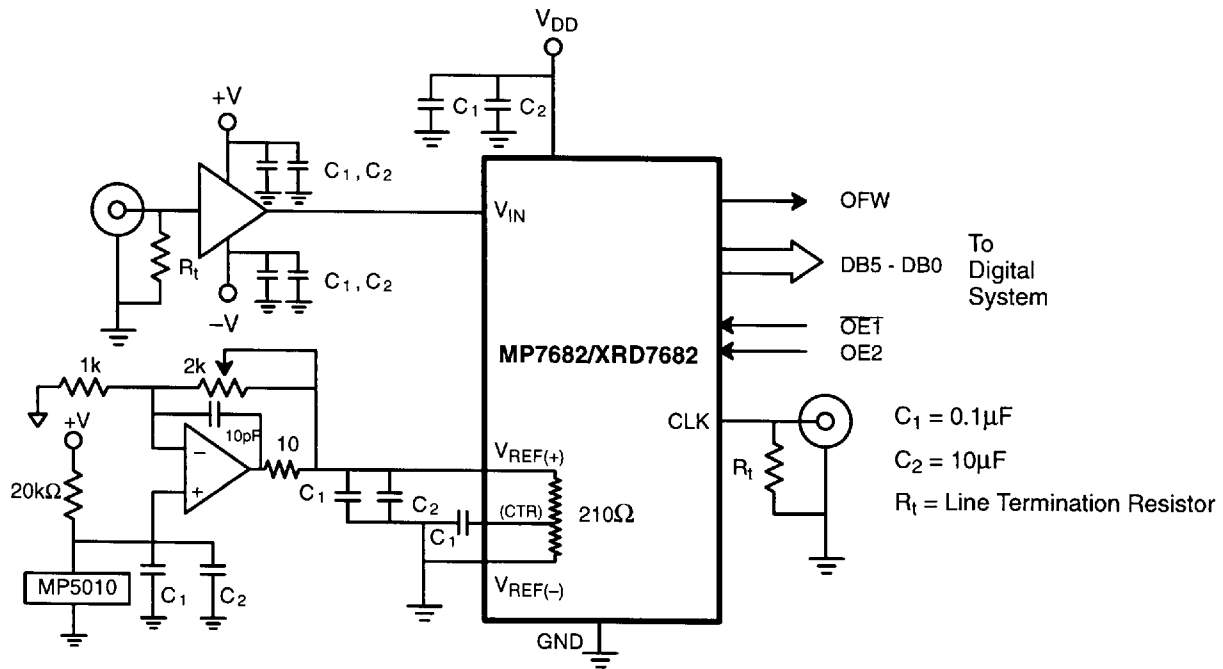
The MP7682/XRD7682 functional equivalent circuit is shown to help the designer to correctly design the timing of his system. The MP7682/XRD7682 is equivalent to an A/D converter followed by a D-type flip-flop (DFF) with the hold and delay times specified in the electrical characteristics.

If another DFF is to follow the ADC, we recommend that the system latches the data at the negative going edge of the clock. If a latch follows the ADC, the positive half of the clock used as enable signal should guarantee stable output at the end of the enable pulse. At high sampling frequencies ( $F_S > 20$  MHz) the user should verify in his system that the MP7682/XRD7682 digital outputs do not change when the digital logic is trying to latch the data. If this problem occurs it may be necessary to invert the logic state of the input PHASE or to change the edge that latches the data into the external circuitry.

## Reference Voltages

If the input bandwidth is limited to the Nyquist region ( $F_{IN} < F_S/2$ ) then the two reference voltages can be set at any two values between the supplies.  $V_{REF}$  (their difference) can be reduced down to 1.5 volts with minor change in accuracy. If the input bandwidth exceeds  $F_S/2$ , then it is recommended that  $V_{REF}$  be lower than  $V_{DD}/2$ .

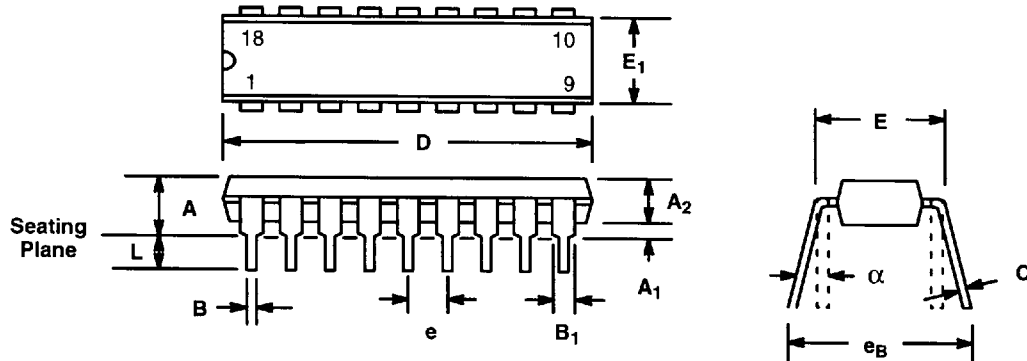




**Figure 12. Typical Circuit Connections**

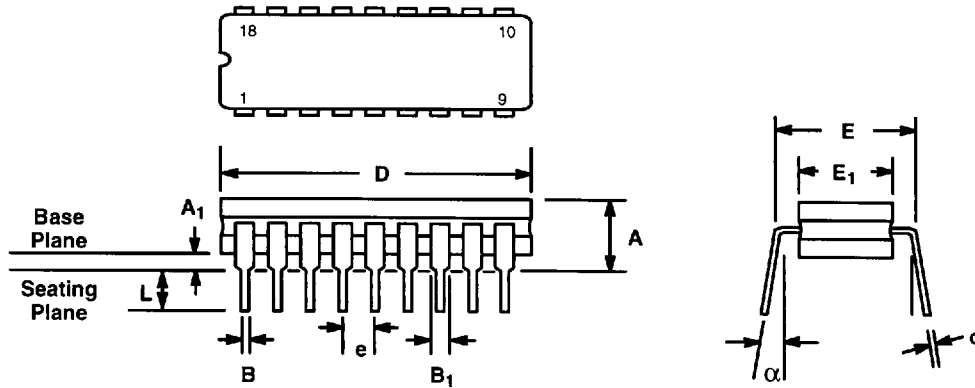
1. All signals should not exceed  $V_{DD} + 0.5\text{ V}$  or  $\text{GND} - 0.5\text{ V}$ .
2. Any input pin which can see a value outside the absolute maximum ratings ( $V_{DD} + 0.5\text{ V}$  or  $\text{GND} - 0.5\text{ V}$ ) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7682/XRD7682 inputs have input protection diodes which will protect the device from short transients outside the supplies range.
3. The PC board design will affect the MP7682/XRD7682 accuracy. Use of wire wrap is not recommended.
4. The analog input signal ( $V_{IN}$ ) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.
5. The analog input should be driven by a buffer op amp with as low an output impedance as possible. The impedance should be less than  $25\Omega$  for clock frequencies above 15 MHz.
6. Ground plane should be substantial. The ground plane should act as a shield for parasitics and not a return path for signals. Separate low impedance ground paths will reduce noise levels.
7. The power supplies and reference voltages should be decoupled with a ceramic ( $0.1\mu\text{F}$ ) and a tantalum ( $10\mu\text{F}$ ) capacitor as close to the device as possible.
8. The digital output should not be driving long wires as the capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used.

## 18 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)



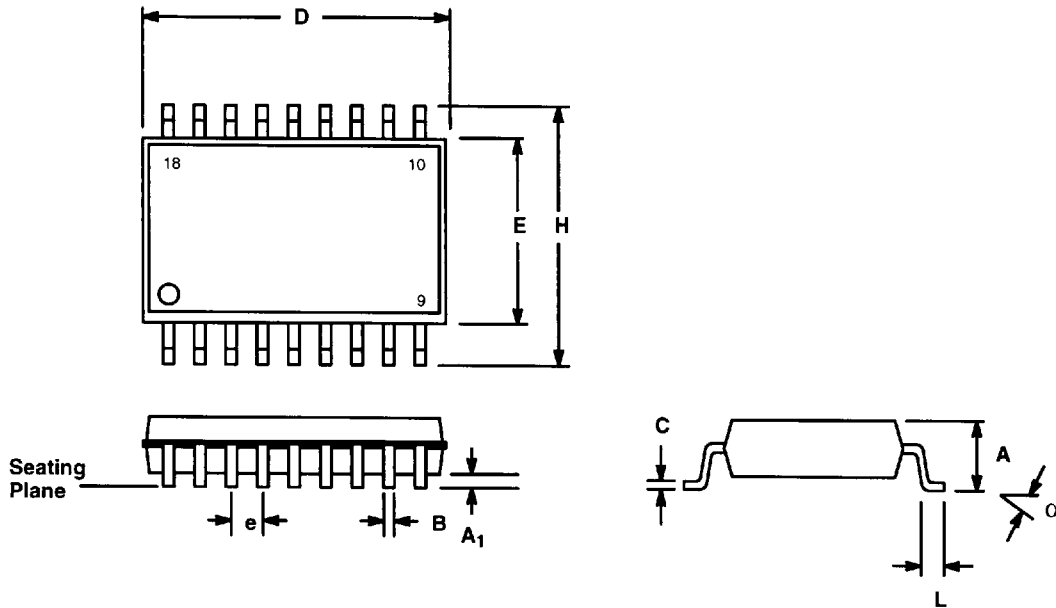
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A <sub>1</sub>	0.015	0.070	0.38	1.78
A <sub>2</sub>	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B <sub>1</sub>	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.845	0.925	21.46	23.50
E	0.300	0.325	7.62	8.26
E <sub>1</sub>	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e <sub>B</sub>	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

**18 LEAD CERAMIC DUAL-IN-LINE  
(300 MIL CDIP)**



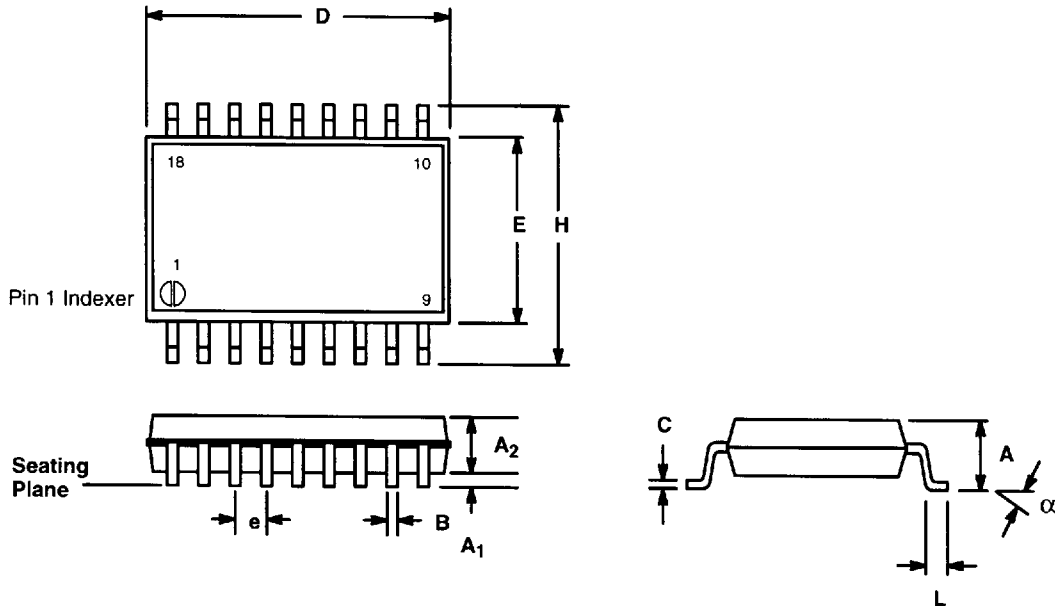
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.100	0.200	2.54	5.08
A <sub>1</sub>	0.015	0.070	0.38	1.78
B	0.014	0.026	0.36	0.66
B <sub>1</sub>	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	0.860	0.960	21.84	24.38
E	0.300 BSC		7.62 BSC	
E <sub>1</sub>	0.250	0.310	6.35	7.87
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
α	0°	15°	0°	15°

## 18 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)



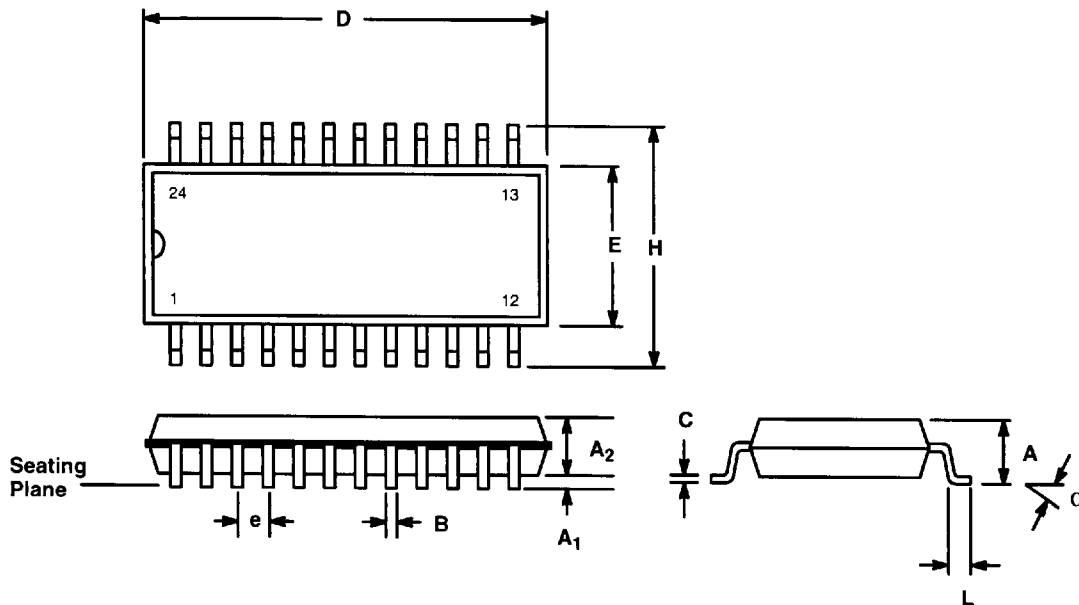
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A <sub>1</sub>	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.447	0.463	11.35	11.75
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

**18 LEAD EIAJ SMALL OUTLINE  
(6.5 mm EIAJ SOP)**



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.80	2.40	0.071	0.095
A <sub>1</sub>	0.02	0.20	0.001	0.008
A <sub>2</sub>	1.80	2.20	0.079	0.087
B	0.30	0.50	0.012	0.020
C	0.13	0.20	0.005	0.008
D	12.50	13.10	0.492	0.516
E	6.30	6.70	0.248	0.264
e	1.27 BSC		0.050 BSC	
H	9.60	10.00	0.378	0.394
L	0.30	0.90	0.012	0.035
α	0°	15°	0°	15°

## 24 LEAD EIAJ SMALL OUTLINE (7.8 mm EIAJ SOP)



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.00	2.40	0.079	0.094
A <sub>1</sub>	0.10	0.30	0.004	0.012
A <sub>2</sub>	1.90	2.10	0.075	0.083
B	0.30	0.50	0.012	0.020
C	0.10	0.20	0.004	0.008
D	15.00	15.50	0.590	0.611
E	7.70	7.90	0.303	0.311
e	1.27 BSC		0.050 BSC	
H	10.20	10.60	0.402	0.417
L	0.20	0.60	0.008	0.024
α	0°	10°	0°	10°