HN62404 Series
HN62424 Series

262144-Word × 16-Bit/524288-Word × 8-Bit CMOS Mask Programmable ROM

HN62404, HN62424 Series is a 4-Mbit CMOS mask-programable ROM organized either as 262144-word x 16-bit or as 524288-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

Features

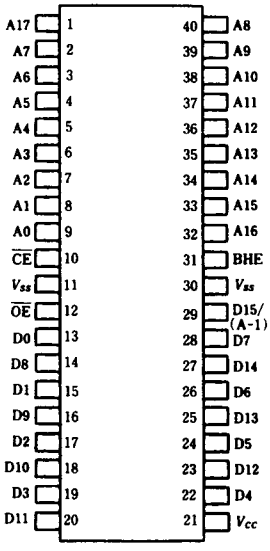
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access ccess time: 150/200 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 µW (typ)
- Byte-Wide or Word-Wide Data Organization(switched by BHE terminal)

Ordering Information

Type No.	Address Access Time	Package
HN62404P	200 ns	600 mil 40-pin
HN62424P	150 ns	plastic DIP
HN62404FP	200 ns	44-pin
HN62424FP	150 ns	plastic QFP

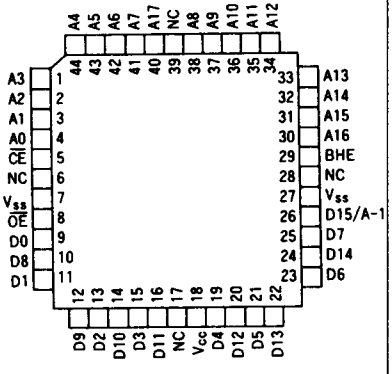
Pin Arrangement

HN62404, HN62424P



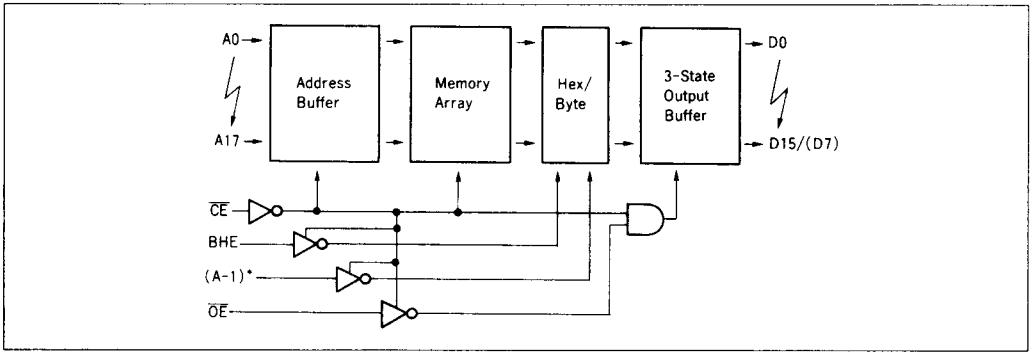
(Top View)

HN62404FP, HN62424FP



(Top View)

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1: A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

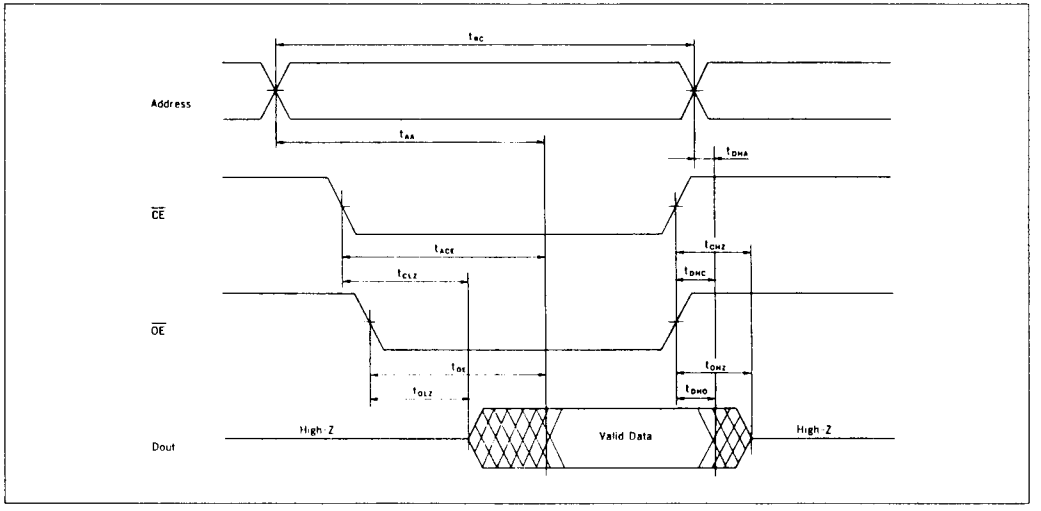
Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	HN62424		HN62404		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
BHE access time	t_{BHE}	—	150	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output Hold Time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns
BHE to Output in Low Z	t_{BLZ}	10	—	10	—	ns

Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

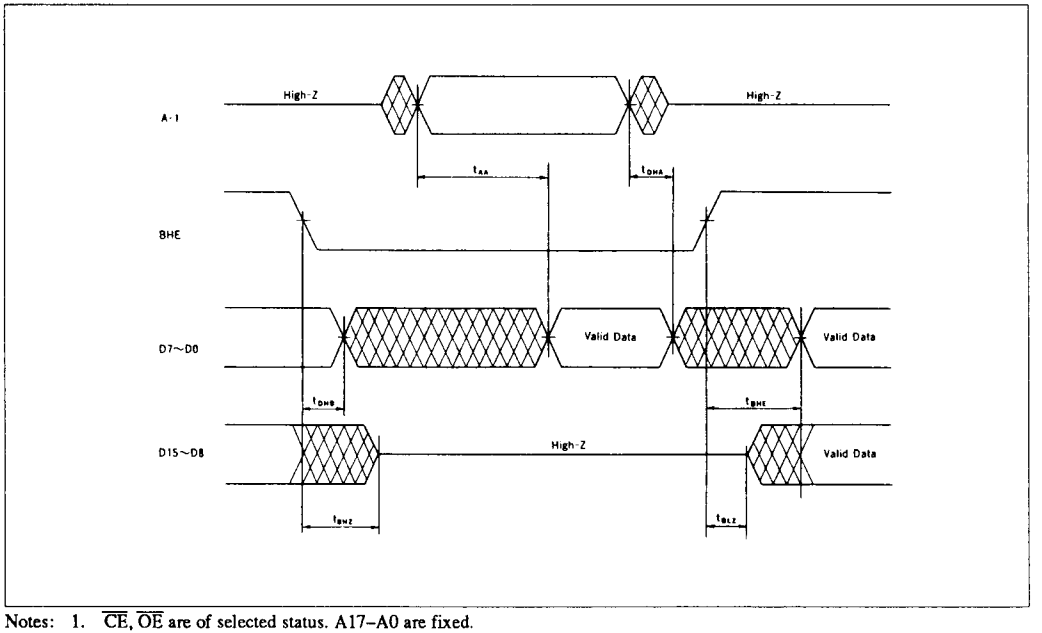
Timing Waveform

Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. CE, OE are of selected status. A17–A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = VIH, CE and OE are of selected state.
At this time, an input signal that is of the inverse phase to the output should not be impressed.