HY93C46

64 × 16-Bit CMOS SERIAL EEPROM

M311201B-APR91

DESCRIPTION

The HY93C46 is a 1,024-bit non-volatile memory organized as 64 registers of 16 bits each. Data can be written into or read out serially by most microprocessors or microcontrollers.

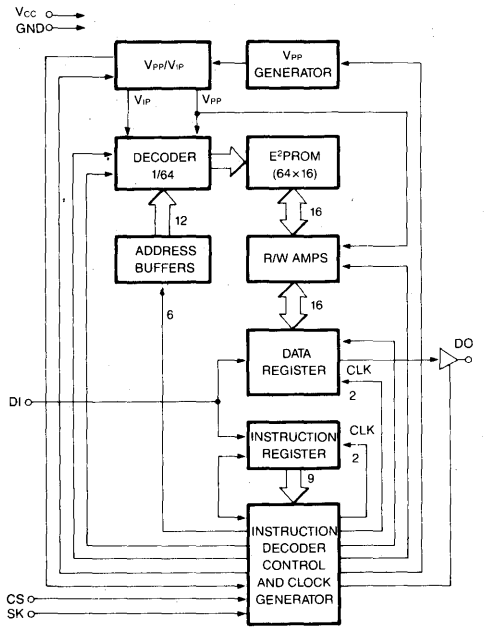
Data is stored in a floating-gate cell with long data retention capability until updated by an erase or write cycle. The HY93C46 has been designed for applications requiring up to ten thousand erase/write cycles per register. Fabricated using advanced CMOS EEPROM technology, the HY93C46 offers very low power consumption. A standby mode is provided by chip select input (CS) to further reduce the power consumption by over 80%.

And to satisfy our customer's requirement, SO package is avaliable.

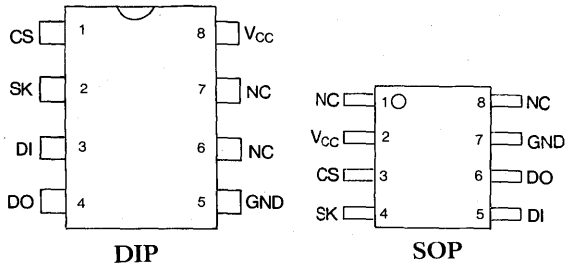
FEATURES

- **CMOS Technology**
- **Low cost**
- **TTL compatible**
- **5V only erase and write(5V ± 10%)**
- **64×16 serial read/write memory**
- **Simple interfacing**
- **Low standby power**
- **Reliable floating-gate technology**
- **Self-timed programming cycle**
- **Device status signal**
- **Compatible with NMC9346/COP495**
- **Long data retention (10 years)**
- **8 pin 300 mil P-DIP and 150 mil SOP**

BLOCK DIAGRAM



PIN CONNECTIONS



PIN DESCRIPTION

SK	Serial Clock ; External user clock shifts data into or out of the HY93C46.
CS	Chip Select ; Enables internal logic when high. Note CS must be brought low between instruction.
DI	Serial Data In ; Data bits and instructions are shifted in through this pin under control of SK and CS.
DO	Serial Data Out ; Data is shifted out from this pin under SK and CS control. DO is active during data output(READ) or while checking status (See WRITE/ERASE Cycles). It is in high impedance state at all other periods.
V_{CC}	Power Supply(+5V)
GND	Ground
NC	No Connection

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ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER		RATING	UNIT
V_{TERM}	Voltage on Any Pin Relative to GND		−0.3 to 6.5	V
T_A	Ambient Operating Temperature	Standard	0 to 70	℃
		Extended	−40 to 85	℃
T_{STG}	Ambient Storage Temperature		−55 to 150	℃

NOTE :

1. Exceeding these ratings could cause permanent damage to the device. These are stress ratings only and functional operation of this device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(T_A=0℃ to 70℃, V_{CC}=5V±10%, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CC}	Operating Current	V_{CC}=5.5V, CS=V_{IH}, SK=V_{IH}		3	mA
	(Program and ERAL modes)	V_{CC}=5.5V		3	mA
I_{CCSB1}	Standby Current TTL Levels	V_{CC}=5.5V, CS=V_{IL}, SK=V_{IH}, DI=V_{IL}, V_{IH}=2.4V, V_{IL}=0.8V		1	mA
I_{CCSB2}	Standby Current CMOS Levels	V_{CC}=5.5V, CS=V_{IL}, SK=V_{IH}, DI=V_{IL}, V_{IH}=5.2V, V_{IL}=0.3V		400	μA
V_{IL}	Input Voltage Low		−0.1	0.8	V
V_{IH}	Input Voltage High		2.0	V_{CC}+1	V
V_{OL}	Output Voltage Low	I_{OL}=2.1mA		0.4	V
V_{OH}	Output Voltage High	I_{OH}=−0.4mA	2.4		V
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{IN}=GND to V_{CC}		10	μA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{OUT}=GND to V_{CC}, CS=0V		10	μA

AC CHARACTERISTICS

(T_A=0℃ to 70 ℃, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SK}	Serial Clock Frequency		0	250	KHz
t_{SKH}	Clock High Time(2)		1		μs
t_{SKL}	Clock Low Time(2)		1		μs
t_{CSS}	Chip Select High to Serial Clock High Delay		200		ns
t_{CSH}	Serial Clock Low to Chip Select Low Delay		0		ns
t_{DIS}	Data Setup Time(WRITE)		400		ns
t_{DIH}	Data Hold Time(WRITE)		400		ns
$t_{PD0, 1}$	Serial Clock to Output Delay	V_{OL}=0.8V, V_{OH}=2.0V, C_L=100PF V_{IL}=0.45V, V_{IH}=2.4V		2	μs
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min. CS Low Time(3)		1		μs
t_{SV}	CS High to Status Valid Delay	C_L=100pF		1	μs
t_{0H}, t_{1H}	Falling Edge of CS to DO High-z			400	ns

NOTES :

2. The SK frequency spec. specifies a minmum SK clock period of 4 μs, therfore in an SK clock cycle t_{SKH}+t_{SKL} must be greater than or equal to 4 μs. e.g., if t_{SKL}=1μs then the minimum t_{SKH}=3μs in order to meet the SK frequency specification.
3. CS must be brought low for a minimum of 1μs (t_{CS}) between consecutive instruction cycles.

INSTRUCTION SET FOR HY93C46

INSTRUCTION	START BIT	OPCODE	ADDRESS	DATA	COMMENTS
READ	1	10	A_5, A_4, A_3, A_2, A_1, A_0		Read Register A_5, A_4, A_3, A_2, A_1, A_0
WRITE	1	01	A_5, A_4, A_3, A_2, A_1, A_0	D_{15}-D_0	Write Register A_5, A_4, A_3, A_2, A_1, A_0
ERASE	1	11	A_5, A_4, A_3, A_2, A_1, A_0		Erase Register A_5, A_4, A_3, A_2, A_1, A_0
EWEN	1	00	11_{XXXX}		Erase/Write Enable
EWDS	1	00	00_{XXXX}		Erase/Write Disable
ERAL	1	00	10_{XXXX}		Erase All Registers
WRAL	1	00	01_{XXXX}	D_{15}-D_0	Write All Registers

FUNCTIONAL DESCRIPTION

The HY93C46 is a small peripheral memory intended for use in applications which require non-volatile storage of data. The HY93C46 is organized as 64 registers of 16 bits. Seven 9-bit instructions control the read, write and erase operations of the device. The HY93C46 operates on 5V(± 10%)supply. The high voltage required for programming is generated by an on-chip circuit which is enabled only during the write, erase, and chip erase modes to prevent spurious programming during other modes. The data out(DO) pin is also used as the status pin during self-timed programming cycles to indicate the ready/busy status of the device. All operations of the HY93C46 begin with the loading of an instruction to the device. Each of the 7 instructions has a logical "1" as a start bit, two op code bits followed by 6 bits of address.(See instruction set table for the HY93C46)

READ

After a read instruction is received, the data stored in the register specified by the address fields of the read instruction is transferred to a 16-bit serial shift register. Data can be shifted out through the DO pin by applying the clock pulses to the Serial Clock (SK) input. Note that a dummy bit(logical"0") precedes the 16-bit data output string. The data at the Data Out pin changes on the low to high transition of the serial clock.

ERASE/WRITE ENABLE AND DISABLE

On power-up, the HY93C46 is set to the programming disable state. In order to program the device, it must be set to the programming enable state by executing an EWEN instruction. After data is written into the device, an EWDS instruction may be executed to prevent accidental programming of the HY93C46. The read instruction, however, is independent of the device's programming state.

ERASE[4]

The registers in the HY93C46 must be erased (all bits set to logical "1") before new data can be written into the registers. After the erase instruction is loaded into the HY93C46, Chip Select(CS) must be pulled low. The falling edge of this signal initiates the self-timed programming cycle. If CS is brought high after a time equal to t_{CS}, the DO pin will indicate the ready/busy status of the device. The DO pin will remain low as long as the HY93C46 is still in the programming mode, and the return of this signal to logical "1" indicates the device is now ready for the next instruction. The register erase instruction (ERASE) will erase the data in the register that is addressed by the address field of the instruction. Chip Erase instruction (ERAL) will cause all registers in the device to be erased.

WRITE[4]

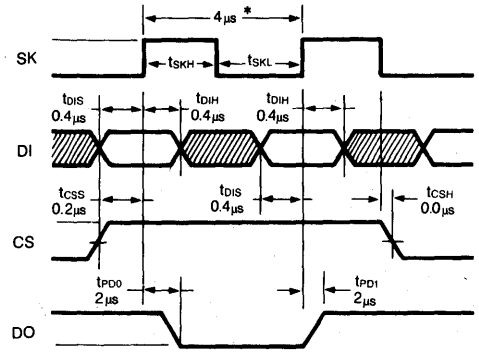
After a write instruction is loaded into the HY93C46 16 bits of data must also be loaded into the device. After the last bit of data is loaded, Chip Select (CS) must be brought low before the next rising edge of the serial clock. The high to low transition of CS will initiate a programming cycle to the register whose address was specified in the write instruction. If CS is again allowed to return to logical "1" after t_{CS}, DO can be examined for the ready/busy status of the device. Note that the register to be written into must have its data previously erased. The chip write instruction (WRAL) is normally used only by the manufacturer to guarantee write/erase endurance of the chip during test.

NOTES :
4. During a programming mode(write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the selftimed programming cycle and starus check.

AC TEST CONDITIONS

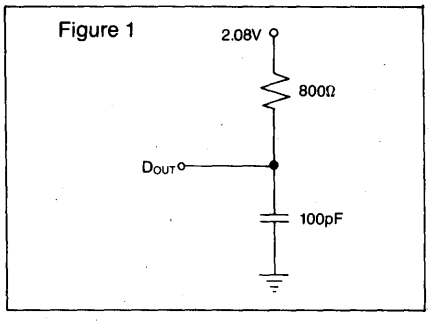
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns Max.
Timing Measurement Levels : Input	1.5V
Output	1.5V
Output Load	See Figure 1

TIMING DIAGRAMS
SYNCHRONOUS DATA TIMING



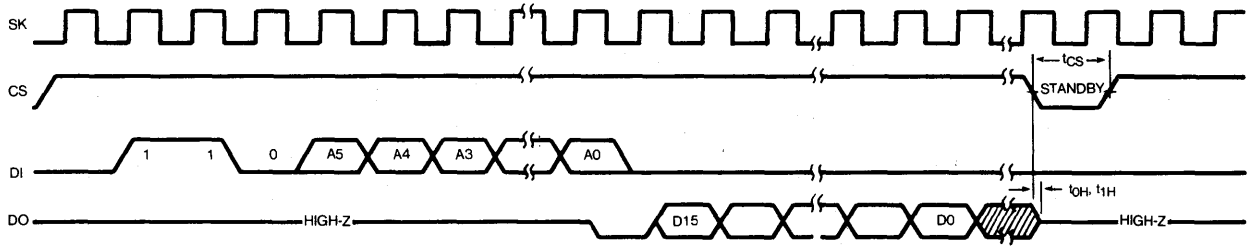
*This is the minimum SK period.

EQUIVALENT
AC TEST CIRCUIT

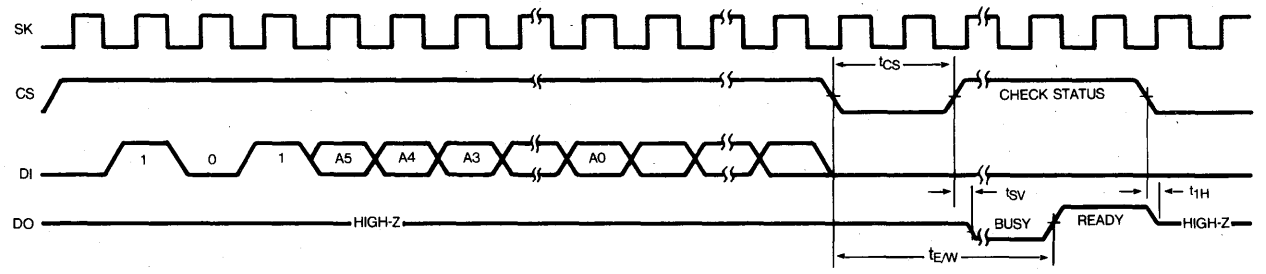


TIMING DIAGRAMS

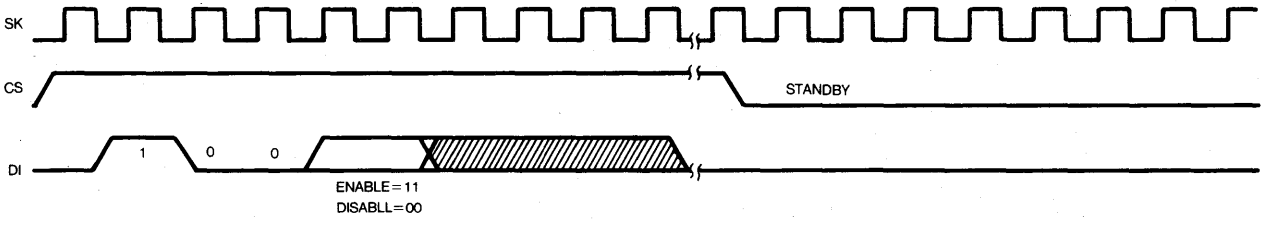
READ



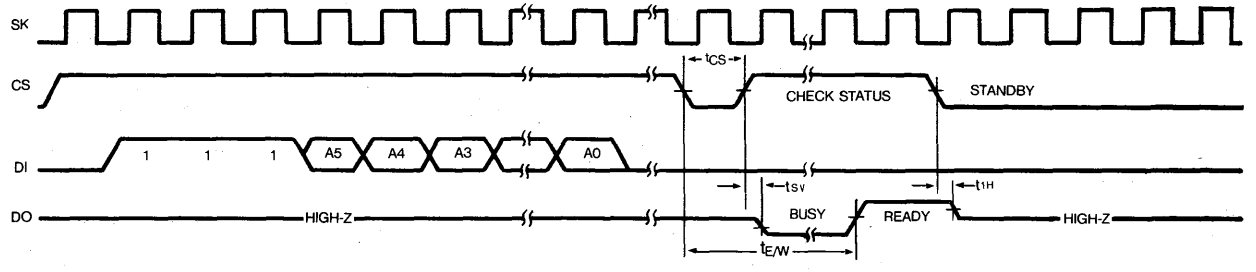
WRITE



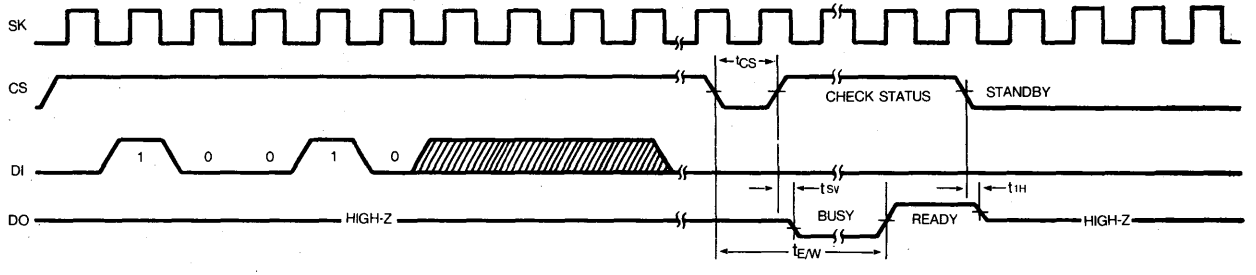
EWEN/EWDS



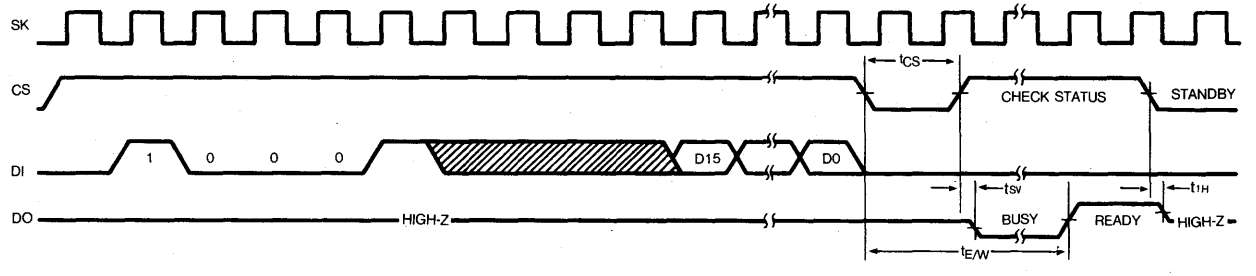
ERASE



ERAL

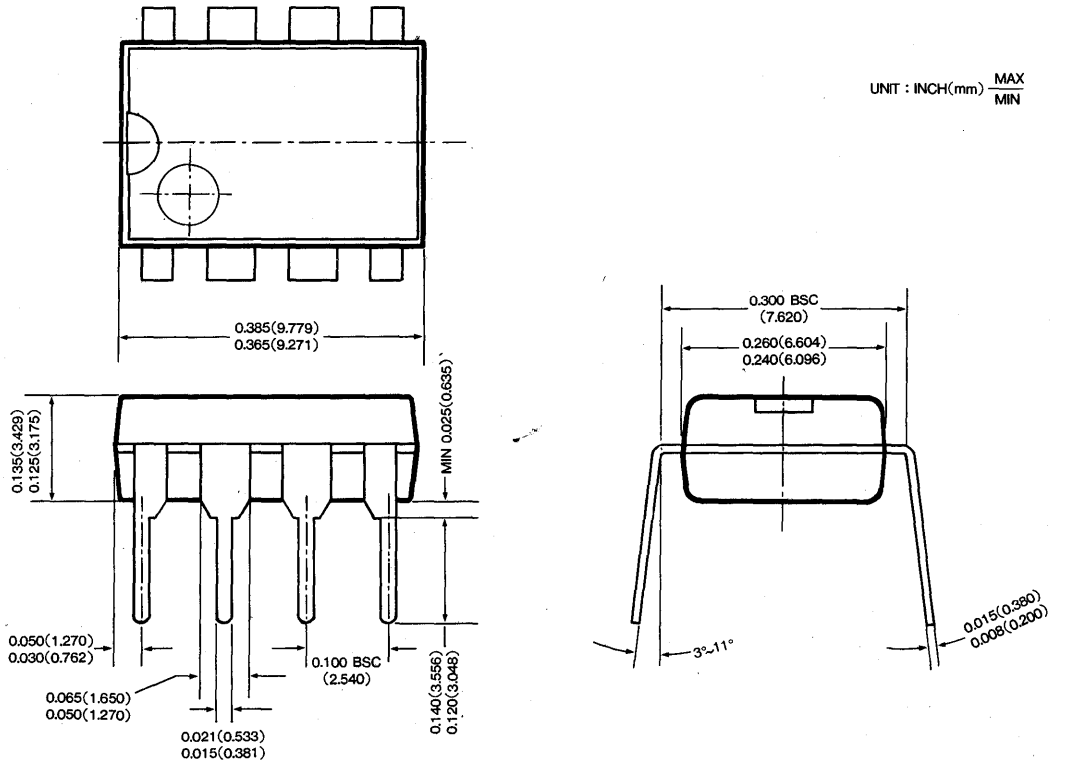


WRAL

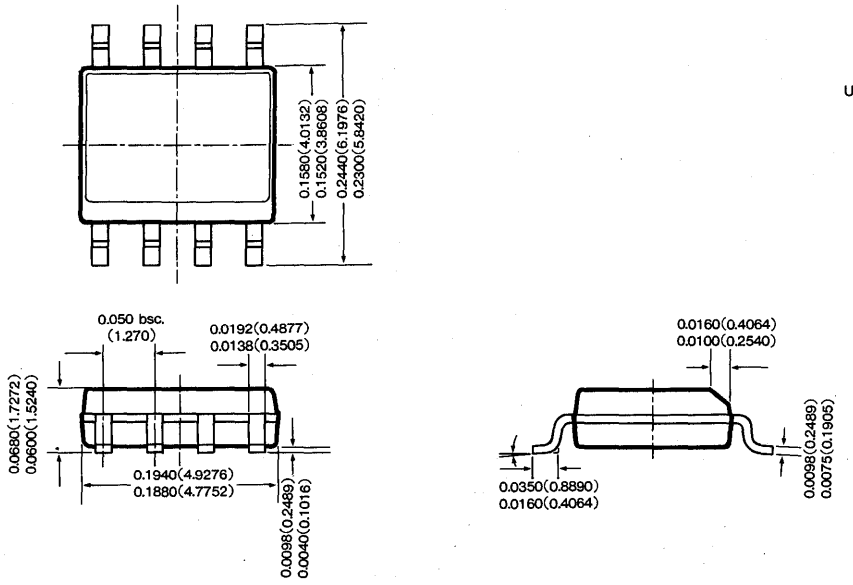


PACKAGE INFORMATION

• 8 PIN PLASTIC DUAL IN LINE PACKAGE−300 MIL



• 8 PIN SMALL OUTLINE PACKAGE−150 MIL



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