

APRIL 1975

DIGITAL 8000 SERIES TTL/MEMORY

DESCRIPTION

The 82S130 (Open Collector Outputs) and the 82S131 (Tri-State Outputs) are Bipolar 2048-Bit Read Only Memories, organized as 512 words by 4 bits per word. They are Field-Programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S130 and 82S131 are supplied with all outputs at logical "0". Outputs are programmed to a logic "1" level at any specified address by fusing a Ni-Cr link matrix.

The 82S130 and 82S131 are fully TTL compatible, and include on-chip decoding and one chip enable input for ease of memory expansion. They feature either Open Collector or Tri-State outputs for optimization of word expansion in bussed organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S130/131, F. For the military temperature range (-55°C to +125°C) specify S82S130/131, F.

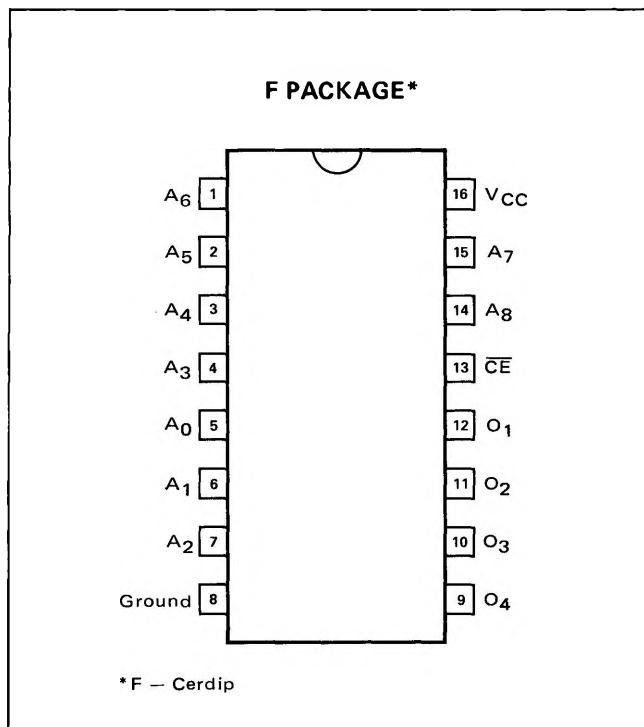
FEATURES

- ORGANIZATION – 512 X 4
- ADDRESS ACCESS TIME:
S82S130/131 – 70ns, MAXIMUM
N82S130/131 – 50ns, MAXIMUM
- POWER DISSIPATION – 0.3mW/BIT TYPICAL
- INPUT LOADING:
S82S130/131 – (-150µA) MAXIMUM
N82S130/131 – (-100µA) MAXIMUM
- ONE CHIP ENABLE INPUT
- ON-CHIP ADDRESS DECODING
- OUTPUT OPTIONS:
82S130 – OPEN COLLECTOR
82S131 – TRI-STATE
- NO SEPARATE "FUSING" PINS
- UNPROGRAMMED OUTPUTS ARE "0" LEVEL
- 16-PIN CERAMIC DIP

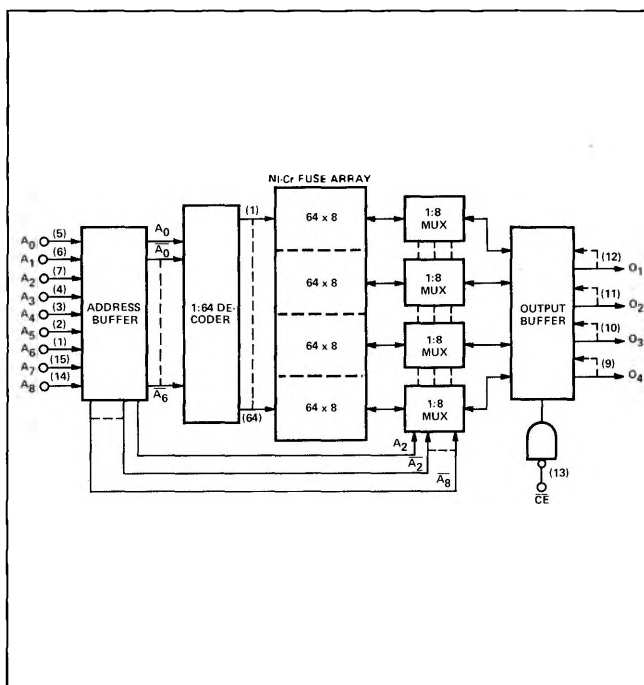
APPLICATIONS

PROTOTYPING/VOLUME PRODUCTION
SEQUENTIAL CONTROLLERS
MICROPROGRAMMING
HARDWIRED ALGORITHMS
CONTROL STORE
RANDOM LOGIC
CODE CONVERSION

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Power Supply Voltage	+7	Vdc
V _{IN} Input Voltage	+5.5	Vdc
V _{OH} High Level Output Voltage (82S130)	+5.5	Vdc
V _O Off-State Output Voltage (82S131)	+5.5	Vdc
T _A Operating Temperature Range (N82S130/131)	0° to +75°	°C
(S82S130/131)	-55° to +125°	°C
T _{stg} Storage Temperature Range	-65° to +150°	°C

ELECTRICAL CHARACTERISTICS

 S82S130/131
 N82S130/131

 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}, 4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$
 $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}, 4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TEST CONDITIONS ¹	S82S130/131			N82S130/131			UNIT
		MIN	TYP ²	MAX	MIN	TYP ²	MAX	
V _{OL} "0" Output Voltage	I _{OUT} = 16mA			0.5			0.45	V
I _{OLK} Output Leakage Current (82S130)	$\overline{\text{CE}} = "1", V_{\text{OUT}} = 5.5\text{V}$			60			40	μA
I _{O(OFF)} Hi-Z State Output Current (82S131)	$\overline{\text{CE}} = "1", V_{\text{OUT}} = 0.5\text{V}$			-60			-40	μA
	$\text{CE} = "1", V_{\text{OUT}} = 5.5\text{V}$			60			40	μA
V _{OH} High Level Output Voltage (82S131)	$\overline{\text{CE}} = "0", I_{\text{OUT}} = -2.4\text{mA},$ "1" STORED	2.4			2.4			V
C _{IN} Input Capacitance	V _{IN} = 2.0V, V _{CC} = 5.0V		5			5		pF
C _{OUT} Output Capacitance	V _{OUT} = 2.0V, V _{CC} = 5.0V		8			8		pF
I _{IL} "0" Input Current	V _{IN} = 0.45V			-150			-100	μA
I _{IH} "1" Input Current	V _{IN} = 5.5V			50			40	μA
V _{IL} "0" Level Input Voltage				.80			.85	V
V _{IH} "1" Level Input Voltage		2.0			2.0			V
I _{CC} V _{CC} Supply Current			120	140		120	140	mA
V _{IC} Input Clamp Voltage	I _N = -18mA		-0.8	-1.2		-0.8	-1.2	V
I _{OS} Output Short Circuit Current (82S131)	V _{OUT} = 0V	-15		-85	-20		-70	mA

SWITCHING CHARACTERISTICS

 S82S130/131
 N82S130/131

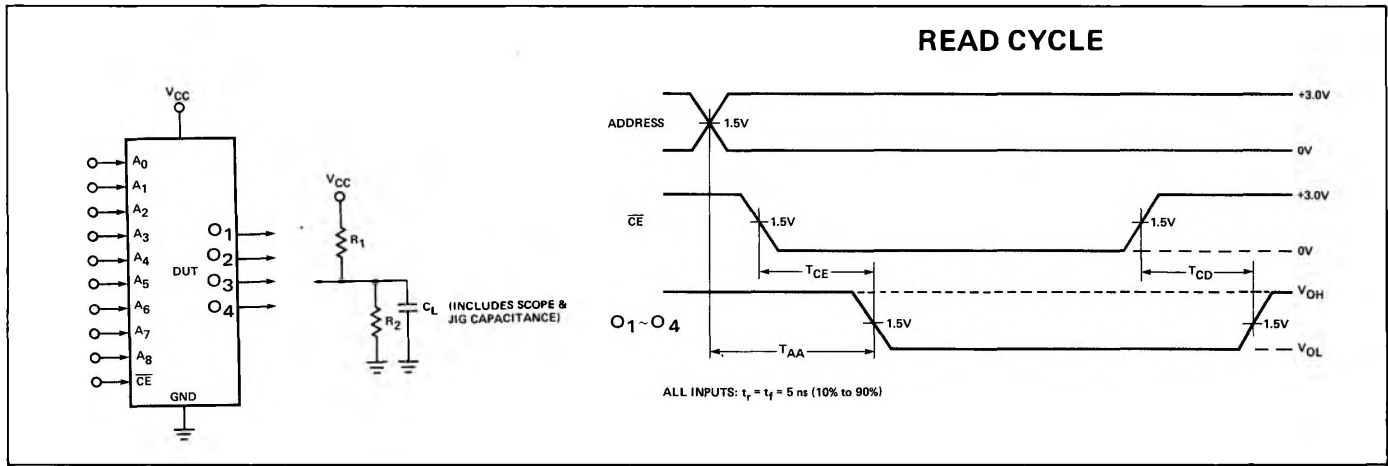
 $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}, 4.5 \leq V_{CC} \leq 5.5\text{V}$
 $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}, 4.75 \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TEST CONDITIONS ¹	S82S130/131			N82S130/131			UNIT
		MIN	TYP ²	MAX	MIN	TYP ²	MAX	
Propagation Delay								
T _{AA} Address to Output	C _L = 30pF		40	70		40	50	ns
T _{CD} Chip Disable to Output	R ₁ = 270Ω		20	30		20	30	ns
T _{CE} Chip Enable to Output	R ₂ = 600Ω		20	30		20	30	ns

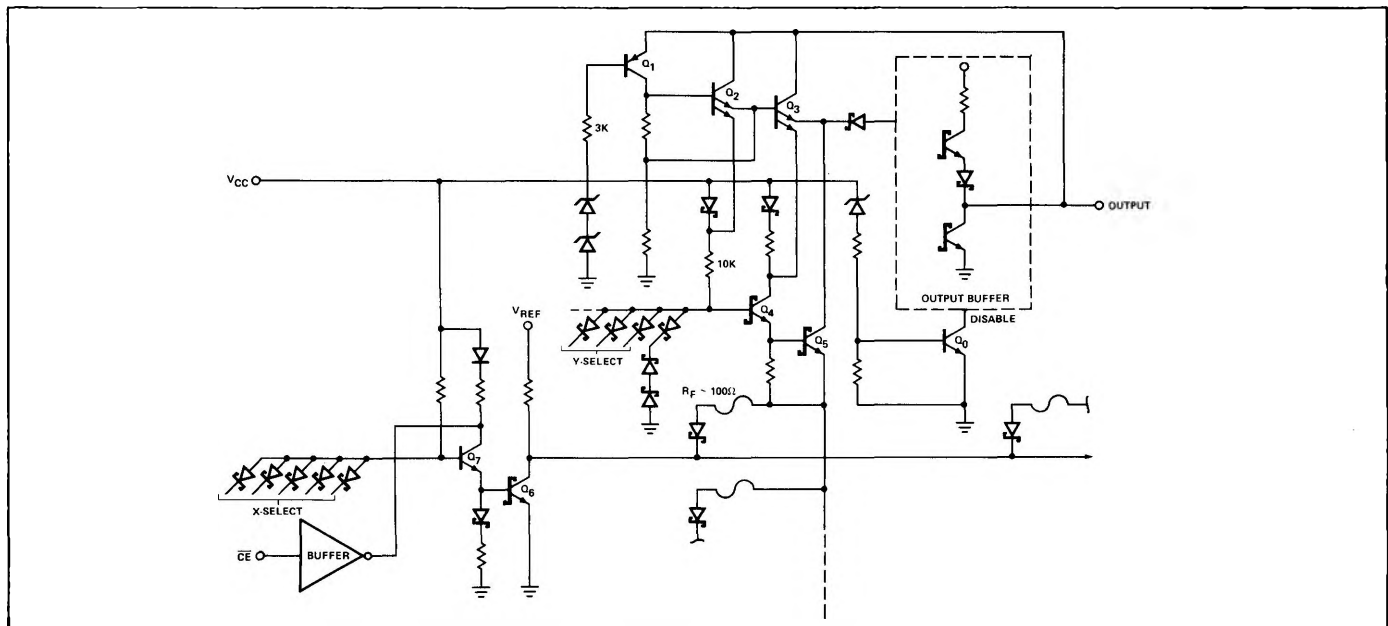
NOTES:

- Positive current is defined as into the terminal referenced.
- Typical values are at V_{CC} = 5.0V, T_A = +25°C.

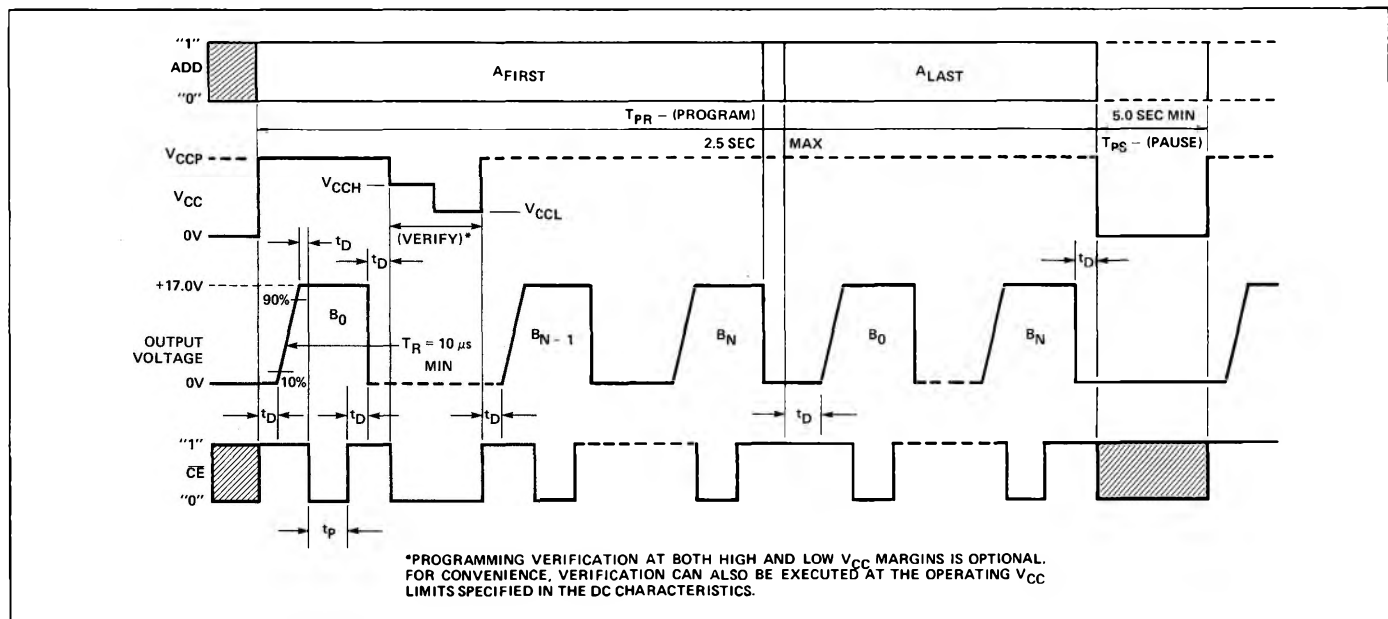
AC TEST FIGURE AND WAVEFORM



TYPICAL FUSING PATH



TYPICAL PROGRAMMING SEQUENCE



PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT		
		MIN	TYP	MAX			
Power Supply Voltage							
V_{CCP}^1	To Program	$I_{CCP} = 350 \pm 50\text{mA}$ (Transient or steady state)		8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit			5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit			4.3	4.5	4.7	V
V_S^3	Verify Threshold			0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	$V_{CCP} = +8.75 \pm .25\text{V}$		300	350	400	mA
Input Voltage							
V_{IH}	Logical "1"			2.4		5.5	V
V_{IL}	Logical "0"			0	0.4	0.8	V
Input Current							
I_{IH}	Logical "1"	$V_{IH} = +5.5\text{V}$				50	μA
I_{IL}	Logical "0"	$V_{IL} = +0.4\text{V}$				-500	μA
V_{OUT}^2	Output Programming Voltage	$I_{OUT} = 200 \pm 20\text{mA}$ (Transient or steady state)		16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	$V_{OUT} = +17 \pm 1\text{V}$		180	200	220	mA
T_R	Output Pulse Rise Time			10		50	μs
t_P	\overline{CE} Programming Pulse Width			1		2	ms
t_D	Pulse Sequence Delay			10			μs
T_{PR}^5	Programming Time	$V_{CC} = V_{CCP}$				2.5	sec
T_{PS}	Programming Pause	$V_{CC} = 0\text{V}$		5			sec
$\frac{T_{PR}^4}{T_{PR} + T_{PS}}$	Programming Duty Cycle					33	%

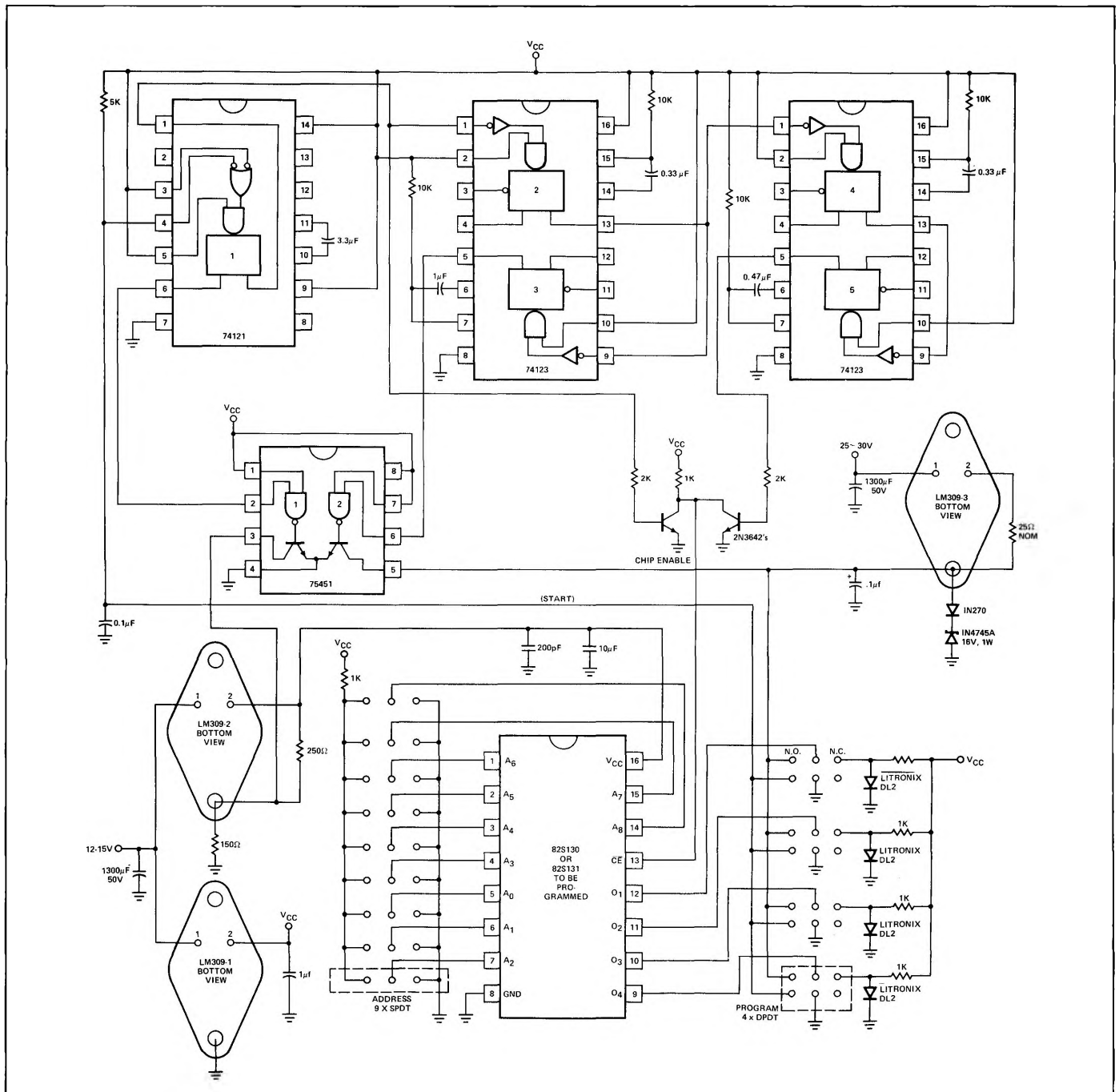
PROGRAMMING PROCEDURE

1. Terminate all device outputs with a $10\text{K}\Omega$ resistor to V_{CC} .
2. Select the Address to be programmed, and raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$.
3. After $10\mu\text{s}$ delay, apply $V_{OUT} = +17 \pm 1\text{V}$ to the output to be programmed. Program one output at the time.
4. After $10\mu\text{s}$ delay, pulse the \overline{CE} input to logic "0" for 1 to 2 ms.
5. After $10\mu\text{s}$ delay, remove +17V from the programmed output.
6. To verify programming, after $10\mu\text{s}$ delay, lower V_{CC} to $V_{CCH} = +5.5 \pm .2\text{V}$, and apply a logic "0" level to the \overline{CE} input. The programmed output should remain in the "1" state. Again, lower V_{CC} to $V_{CCL} = +4.5 \pm .2\text{V}$, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to $V_{CCP} = 8.75 \pm .25\text{V}$, and repeat steps 3 through 6 to program other bits at the same address.
8. After $10\mu\text{s}$ delay, repeat steps 2 through 7 to program all other address locations.

NOTES:

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 4ms.
5. On the first programming attempt (from cold start) a maximum limit of 5 sec. is allowed. In most cases, depending on the truth table, this will decrease total programming time.

N82S130/131 MANUAL PROGRAMMER



TIMING SEQUENCE

